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REMARKS

Claims 1-26 and 36-55 are pending.

Upon entry of this amendment, claims 1-142 will be pending, since this amendment presents new claims 56-142.

Claims 53-55 stand withdrawn. The applicant is disputing the withdrawal of claims 53-55 via a petition previously filed a decision on which is pending.

Claims 1-26, 37, and 39-52 stand allowed.

Claims 36 and 38 stand rejected. This application is currently under appeal due to the rejections of claims 36 and 38.

This amendment presents amended versions of claims 36, 37, and 39, and adds new claims 56-142.

I note that the previously submitted amendment presenting claims 56-58 has not been entered, and therefore I represent claims 56-58 as status "New". This amendment represents the same claims 56-58 as the un-entered amendment.

New dependent claims 56 and 57 both depend from claim 36.

New claims 58-61 are modeled after claims 39 and 53, but more broadly define the second layer of the gate insulator structure. Therefore, these claims are supported by the specification for the same reasons claims 39 and 53 are supported.

New claims 62 and 63 define the quiescient state leakage current limitation noted in the specification (1) by the sentence spanning pages 5-6 (referring to quiescient state leakage current of many micro amps) and (2) page 8 liens 9-10 (specifying leakage currents approaching 10 to the minus 12 amp). Therefore, these claims are supported by the specification.

New claims 64-117 are identical to 1-26 and 36-63, except that new claims 64-117 are not limited to "enhancement mode" transistors. Claims 64-117 are supported by the specification for the same reasons applicable to claims 1-26 and 36-63. Moreover, these claims are supported by the discussion in the specification of both enhancement and depletion mode transistors, for example, in the FIELD OF THE INVENTION SECTION's sole paragraph and page 3 line 1 of the substitute specification.

New dependent claim 118 defines depletion mode transistors. Claim 118 is supported by the discussion in the specification of both enhancement and depletion mode transistors, for example, in the FIELD OF THE INVENTION SECTION's sole paragraph and page 3 line 1 of the substitute specification.

New claims 119-142 are copied exactly from claims 1-24 published in PGP 20030137018 published July 24, 2003, which is a U.S. patent publication of U.S. application number (series code and serial number) 10/051494 naming as inventors "Passlack, Matthias; (Chandler, AZ) ; Medendorp, Nicholas William JR.; (Goleta, CA) " and listing as the correspondence address: MOTOROLA, INC., CORPORATE LAW DEPARTMENT - #56-238, 3102 NORTH 56TH STREET, PHOENIX, AZ 85018 US.

This specification obviously supports the GaAs substrate, interface layer of gallium oxide, and second layer of Gallium Gadolinium Oxide defined in independent claims 119 and 127 (copies of claims 1 and 8 in the 10/051494 application). See for example substitute specification page 5 line 19 (GaAs substrate), page 4 lines 19-22 (gallium oxide interfacial layer), and page 5 lines 1-2 and and page 9 line 17 (disclosing Gadolinium as the rare earth of the Gallium Rare Earth Oxide second layer).

The examiner should review the MPEP guidance regarding claims copied from a pending application and 37 CFR 1.604, and proceed accordingly, in view of this notice of claims copied from a pending application.

In addition, the examiner of this application should place a note in the other application (10/051494), or otherwise notify the examiner of the 10/051494 since this application has a filing date (8/10/2000) that precedes the 10/051494 application's filing date (1/18/2002), by 17 months, and this application has a priority claim to 5/4/2000, which precedes the 10/051494 application's filing date by 20 months. Moreover, the disclosure of this application was published as PCT/US01/25150 in publication WO 02/15233 on August 10, 2001, which date was 5 months prior to the filing date of the 10/051494 application. Accordingly, the examiner of the 10/051494 application should be notified of the existence of this application and WO 02/15233 prior to examining the 10/051494 application.

Claim 36 is amended to delete alternatives of AlGaAs and InGaP in the compound

semiconductor wafer structure, leaving only the InGaAs, AlInAs, and InP alternatives. This amendment is supported by the substitute specification page 5 line 18 et seq, which states that:

> In another preferred embodiment, the compound semiconductor heterostructure comprises an $In_yGa_{1-y}As$, $Al_xIn_{1-x}As$, and InP compound semiconductor heterostructure and n-type and/or p-type charge supplying layers which are grown on an InP substrate

New claim 56 depends from claim 36 and recites that "The transistor of claim 36 wherein said compound semiconductor wafer structure comprises an InP upper spacer layer." This limitation is supported by original claims 27, 28, 30, 32, and 33, particularly original claims 27 and 33, which state that:

> 27. An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:
>
> a compound semiconductor wafer structure having an upper surface;
>
> a gate insulator structure positioned on upper surface of said compound semiconductor wafer structure;
>
> a stable refractory metal gate electrode positioned on upper surface of said gate insulator structure;
>
> source and drain ion implants self-aligned to the gate electrode; and
>
> source and drain ohmic contacts positioned on ion implanted source and drain areas,
>
> wherein the compound semiconductor wafer structure comprises a wider band gap spacer layer and a narrower band gap channel layer.
>
> 28. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the wider band gap spacer layer is positioned between the gate oxide layer and the narrower band gap channel layer.
>
> 30. An enhancement mode metal-oxide-compound semiconductor field

effect transistor as claimed in claim 27 wherein the wider band gap spacer layer comprises either $Al_xGa_{1-x}As$, InP, or In_zGa_{1-z} P or a combination thereof.

32. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the narrower band gap channel layer is positioned between the wider band gap spacer layer and a buffer layer.

33. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the narrower band gap channel layer comprises $In_yGa_{1-y}As$.

New claim 57 depends from claim 14 and is supported by original claim 34's recitation of InGaP as being one alternative for the "layer being positioned on upper surface of a compound semiconductor substrate." and in original claim 30's recitation "An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the wider band gap spacer layer comprises either AlxGa1-xAs, InP, or InzGa1-z P or a combination thereof."

In response to the restriction requirement, the applicant maintains that requirement is improper. The applicant's petition challenging that restriction is pending decision.

In response to the objection to the drawings for not showing a "complementary metal oxide compound semiconductor integrated circuit", the applicant proposes adding new Fig. 3 and a citation to Fig. 3 in the Brief Description of the Figures section of the specification. A formal Fig. 3 is attached to this amendment. This amendment proposes a suitable amendment to the specification. Fig. 3 contains no new matter. The examiner's proposal to show that structure in Fig. 1 is not feasible, since Fig. 1 shows the microstructure of one transistor, not an IC. Showing an IC would be incompatible with showing a layered structure of one transistor. Fig. 3 shows a complementary IC, i.e., one that includes n and p type transistors, thereby meeting the requirement imposed by the examiner since it shows the "complementary IC" and Fig. 1 shows the metal oxide structure of each IC.

Also filed with this amendment please find the following papers:

Paper marked attachment 5, which is the now published version of Chapter 12 in

"Gallium Oxide on Gallium Arsenide Atomic Structure, Materials, and Devices" in III-V Semiconductor Heterostructures: Physics and Devices, edited by W. Z. Cai, Published by Research Signpost, India, ISBN: 81-7736-170-8. The pre-publication version was submitted with Dr. Braddock's second 37 CFR 1.132 declaration.

Paper marked attachment 6, which is a copy of Becke et al. "Gallium Arsenide MOS Transistors" Solid State Electronics, Vol 8 pp. 813-823 (1965). This paper is referred to in Dr. Johnson's 37 CFR 1.132 declaration.

Paper marked attachment 7, which is a copy of an eight page facsimile (with pages hand numbered in the upper right hand corner) including cover letter from Mark Johnson (1 page), 37 CFR 1.132 declaration of Mark Johnson (4 pages numbers consecutively numbered at the bottom 1 to 4), and copy of Fountain et al, "Demonstration of an n-Channel Inversion Mode GaAs MISFET" (3 pages).

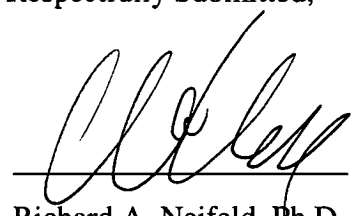
Paper marked attachment 8, which is a copy of a printout of www.accuratus.com/fused.html (2 pages) showing volume resistivity of fused SiO2 as greater than ten to the tench Ohm-cm.

When these papers are entered, the examiner should consider Dr. Johnson's declaration which explains why the Passlack patent '718 does not disclosure or suggest either a MOS FET or a gate insulator structure.

In view of the comments in the Supplemental Appeal Brief and the Second 37 CFR 1.132 declaration of David Braddock, and attachments 1-3 to the Supplemental Appeal Brief, and the petition to remove withdrawal of claims 53-55, and Dr. Johnson's declaration and supporting documents, this application, including claim 53-118, are believed to be in condition for allowance, which is requested.

Since this application has a much earlier effective filing date that the application from which claims 119-142 are copied, this application should be issued, the other application should not be issued, and then an interference declared - - assuming the claims in the other application are found otherwise allowable. See MPEP chapter 2300.

Respectfully Submitted,

7/19/04 

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LIST OF ATTACHMENTS

Attachment 5- Published version of Chapter 12 in "Gallium Oxide on Gallium Arsenide Atomic Structure, Materials, and Devices" in III-V Semiconductor Heterostructures: Physics and Devices, edited by W. Z. Cai, Published by Research Signpost, India, ISBN: 81-7736-170-8.

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12 Gallium oxide on gallium arsenide: Atomic structure, materials, and devices

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Abstract

This study pertains to aspects of deposited gallium oxide films on gallium arsenide including (1) atomic surface and interface structure, (2) deposition technique, (3) film and interface properties, and (4) field effect transistor applications. Ga_2O_3 films are deposited by effusive evaporation from a polycrystalline Ga_2O_3 source onto the GaAs(001)-(2x4) surface in ultra-high vacuum. The first monolayer of Ga_2O forms a charge balanced (2x2) surface order with a crystalline interface that is electronically unpinned. Further deposition proceeds via the formation of amorphous bulk Ga_2O_3. We review the structural and electrical properties of Ga_2O_3 films and Ga_2O_3 -GaAs interfaces. Finally, a GaAs based enhancement-mode heterostructure MOSFET is discussed and a performance comparison to prior art is presented.

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1 Introduction

The quest for III-V gate oxides has been fueled by scientific curiosity and commercial opportunity for almost four decades. More recently, the demand for III-V semiconductors in high volume applications such as wireless and fiber optic communications has sparked even stronger interest in III-V based metal-oxide-semiconductor (MOS) field effect transistors (FET); the past and present lack of III-V MOSFET devices has limited functionality, scalability, performance, and market acceptance of III-V technologies.

Excellent reviews of early gate insulator research on III-V semiconductors were published by W.F. Croydon and E.H.C. Parker [1] and C.W. Wilmsen [2] in 1982 and 1985, respectively. The conclusions of almost 20 years of effort in the field were not encouraging: attempts at adopting the wildly successful thermal oxidation technique of silicon had failed and insulator deposition techniques did not look more promising [1]-[10]. Consequently, the field had been nearly abandoned. However, the pioneering work by Spicer [11], Pianetta [12] and others had greatly advanced the understanding of III-V semiconductor surface reactivity and would later support the foundation of modern III-V MOS technology concerning the requirement of surface preparation under ultra-high vacuum conditions.

When Callegari et al. reported on the first deposition of gallium oxide thin films on GaAs in 1988 [13], the evidence of Fermi level unpinning was spotty at best and the deposition technique was questionable; the oxide film was prepared by gallium metal deposition in an oxygen plasma. In fact, the authors attributed the suggested Fermi level unpinning to hydrogen and nitrogen plasma treatments rather than to the formation of a gallium oxide-GaAs interface. This was in agreement with conventional wisdom at the time: it was speculated that any material containing oxygen causes Fermi level pinning (pp. 197-198 in [2]), a hypothesis apparently substantiated by Spicer's earlier observation of Fermi level pinning at an oxygen exposed GaAs surface [11].

Work on gallium oxide deposition on GaAs was accelerated at AT&T Bell Laboratories in early 1993. The motivation for this effort is intuitive--it was thought that an interface comprising similar materials is more likely to exhibit an unpinned Fermi level compared to an interface consisting of more dissimilar materials. Since existing gallium oxide deposition techniques [13]-[15] were considered to be incompatible with the requirements of oxide deposition onto a GaAs surface, electron beam evaporation from a high purity, single crystal gadolinium gallium garnet ($Gd_3Ga_5O_{12}$) was introduced [16], [17]. Initially, G. Zydzik deposited gallium oxide films onto GaAs substrates. However, Fermi level unpinning was only observed later when M. Hong and J.P. Mannaerts deposited oxide films on freshly grown GaAs(001) surfaces using in-situ molecular beam epitaxy (MBE) [18]-[23]. Most important, accumulation and inversion in n- and p-type capacitors were demonstrated [18]. This unequivocally established the requirement of ultra-high vacuum for Fermi level unpinning at the oxide-GaAs interface. Early applications included mirror passivation of high power 980 nm pump laser [24], [25].

Although the demonstration of inversion/accumulation at oxide-GaAs interfaces [18] represented an impressive engineering feat, the underlying fundamental mechanism of Fermi level unpinning remained elusive. The matter was further complicated by the presence of Gd in the oxide films manufactured at AT&T Bell Laboratories [18], [22]. In addition, it was found that in-situ MBE of other oxides such as aluminum oxide, silicon

oxide, and magnesium oxide resulted in Fermi level pinning [20]. Obviously, the atomic level structure of the oxide-GaAs interface and its associated electrical properties had to move to center stage: to reveal the interface's fundamental properties became imperative for further technology advancement.

This paper represents a first comprehensive, seminal work on unpinned oxide-GaAs interfaces commencing with fundamental atomic level interface studies and concluding with the demonstration of an enhancement mode heterostructure MOSFET. The foundation of this work is the unique property of gallium oxide to unpin the interface Fermi level on GaAs. All aspects of Ga_2O_3 deposition are discussed: atomic structure, physics, chemistry, materials, characterization, manufacturing, and device processing. Significant progress in experimental and theoretical methods, equipment, and manufacturing techniques have led to fundamental advancements and discoveries as further discussed below.

The introduction of effusive evaporation from a crystalline Ga_2O_3 source provides a high purity molecular gallium oxide beam and enables the reproducible manufacture of smooth, amorphous Ga_2O_3 films forming atomically abrupt interfaces with GaAs(001) [26] (Section 3). Scanning tunneling microscopy, scanning tunneling spectroscopy, low energy electron diffraction, and Auger electron spectroscopy supported by density functional calculations reveal that a monolayer of Ga_2O molecules forms a charge balanced (2x2) surface order on GaAs(001) that is electronically unpinned [27] (Section 2). The amorphous oxide films are stoichiometric (Ga_2O_3) and of high volume density. The atomically abrupt interface is thermally stable [28] and characterized by low interface recombination velocity and interface state density [29]. In analogy to the SiO_2-Si system, hydrogen atoms are found to passivate defects at as-deposited Ga_2O_3-GaAs interfaces [30]. A photoluminescence intensity technique enables interface optimization [31] and, in combination with standard capacitance-voltage (C-V) measurements, virtually eliminates common pitfalls in insulator-III-V semiconductor interface characterization (Section 4). The effort culminates in the first demonstration of a functional enhancement mode GaAs based MOSFET. The 0.6 μm self-aligned p-channel heterostructure MOSFET exhibits a maximum dc transconductance g_m of 51 mS/mm, an improvement of more than two orders of magnitude over previously reported results. A complete and manufacturable process flow and 66% of theoretical performance are demonstrated [32] (Section 5).

The authors believe that the discussed technology constitutes a milestone in the development of commercially viable III-V MOSFETs. The presented technology has its deficiencies and challenges remain.

2 Atomic surface and interface structure

We first discuss the basic chemistry and physics of the oxide-semiconductor interface. To ensure an unpinned Fermi level, the atomic structure of the interface must be controlled. Through the aid of scanning tunneling microscopy (STM), scanning tunneling spectroscopy (STS), low energy electron diffraction (LEED), and Auger electron spectroscopy (AES), we are able to directly show which adsorption sites provide an unpinned interface Fermi level.

A clean GaAs(001)-(2x4) surface reconstruction is obtained by thermally desorbing an arsenic capping layer from a GaAs wafer grown by molecular beam epitaxy (MBE) in

an ultra-high vacuum (UHV) chamber. The clean surface is confirmed by AES, LEED, and STM. A filled-state STM image of the clean surface taken with a bias of -3 V and a constant tunneling current of 0.2 nA is shown in Fig. 1. In STM, the electronegative arsenic atoms image as bright features and the electropositive gallium atoms image as dark features. As seen in the ball-and-stick diagram in Fig. 1, the bright rows along the [$\bar{1}$ 10] azimuth consist of two arsenic dimmers that bond in the same direction as the row [33], [34]. An additional arsenic dimer resides in the trough of each unit cell, but this dimer is not imaged in STM due to the exponential tunneling dependence on the tip-sample separation. Also present in the STM image in Fig. 1, and represented in the ball-and-stick diagram, are arsenic dimer vacancies. These sites are formed during the thermal decapping procedure.

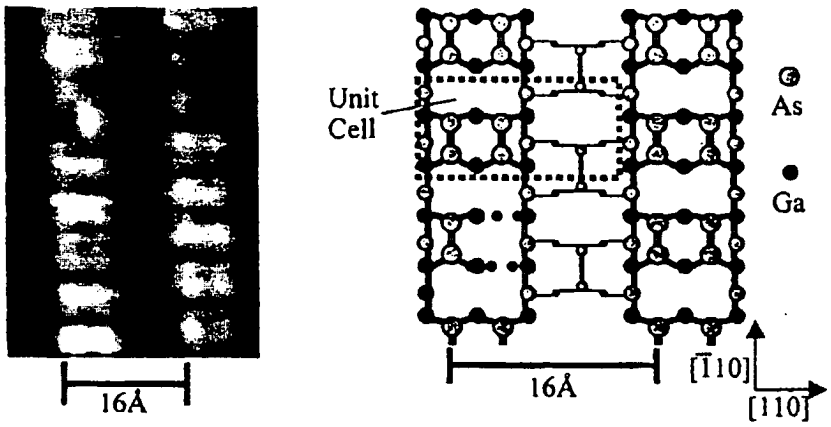

Figure 1. A filled state STM image (left) of a clean GaAs(001) (2x4) surface reconstruction taken at V = -3 V and I = 0.2 nA. The clean surface is comprised of three arsenic dimers per unit cell as seen in the unit cell specified in the ball-and-stick diagram (right). The legend in the lower right corresponds to both the STM image and the ball-and-stick diagram.

After the confirmation of a clean GaAs(001)-(2x4) surface reconstruction, the surface is dosed in-situ at an elevated surface temperature with $Ga_2O_{(g)}$. The $Ga_2O_{(g)}$ molecules are produced from the sublimation of polycrystalline Ga_2O_3 (see also Section 3). The polycrystalline Ga_2O_3 sublimates as $Ga_2O_{(g)} + O_{2(g)}$ [35]-[37]. The sticking probability of $O_{2(g)}$ is about six orders of magnitude lower than that of $Ga_2O_{(g)}$ at 25°C [38]; therefore, it can be assumed that only $Ga_2O_{(g)}$ sticks to the clean surface. A filled state STM image at submonolayer coverage of Ga_2O/GaAs(001) taken with a sample bias of -1.5 V and a tunneling current of 0.2 nA is shown in Fig. 2. In this image, the gallium atoms in the Ga_2O molecule image as the brightest features, despite gallium being an electropositive atom, due to their height above the arsenic atoms in the original arsenic dimer row. The oxygen atoms are not imaged because the electronic states associated with them reside well below the valence band maximum (VBM) [38]. From this image, it can be seen that Ga_2O molecules insert into two arsenic dimers on top of the original arsenic dimer row. The ball-and-stick diagram in Fig. 2 shows the atomic placement of the Ga_2O insertions. Ga_2O bonding is not observed in the trough due to the lack of arsenic dimer pairs.

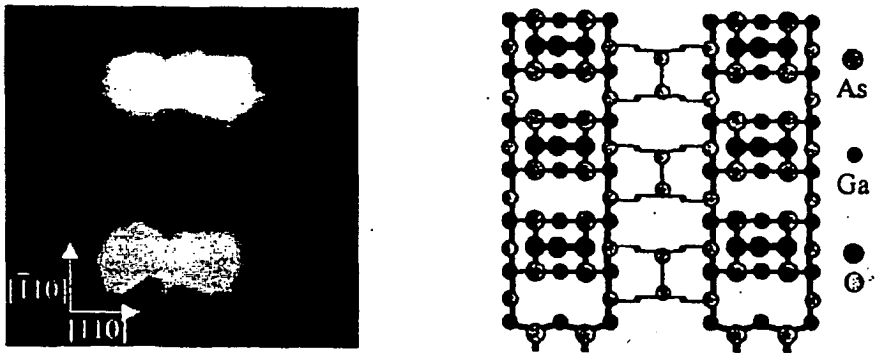

Figure 2. Filled state STM image of two Ga_2O molecules inserted into the As dimer row taken at V = -1.5 V and I = 0.2 nA (left). The brightest features in the image are the Ga_2O molecules inserted into the As dimers, and the black region is the trough. The legend in the lower left describes both the STM image and the ball-and-stick diagram (right).

Line scan analysis from both the clean GaAs(001)-(2x4) surface and from the same surface with Ga_2O inserted into the row arsenic dimers can be seen in Fig. 3. From the top half of Fig. 3, line scans are taken along the [110] direction (across the dimer row). The clean surface shows the row width to be 4 Å, whereas the row width on Ga_2O/GaAs is measured to be 5 Å along the Ga_2O molecule. Line scans along the arsenic dimer row ([$\bar{1}$10]) show an even more pronounced difference between the clean surface and the surface formed upon deposition of Ga_2O. The first major difference is the apparent depth between the two peaks that are spaced 8 Å apart. The clean surface has an apparent depth of 0.2 Å, whereas the Ga_2O inserted site has an apparent depth of 0.4 Å. This difference is attributed to the height difference between the gallium and arsenic atoms and the ability of the arsenic atoms' electrons to more readily tunnel into the tip. The other major difference between the two line scans is the 4 Å spacing along the dimer row of the clean surface showing the two arsenic dimer atoms versus the 2 Å spacing along the Ga_2O inserted site showing only the single gallium atom. This line scan clearly shows the difference between the two sites.

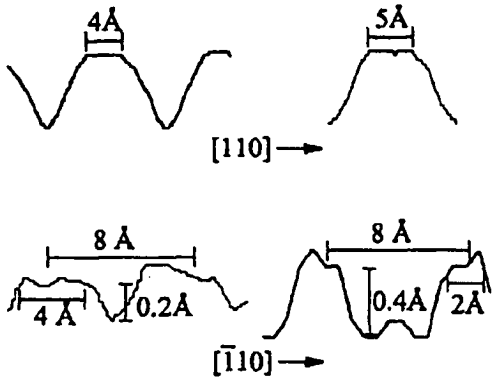

Figure 3. Line scans of the As dimer rows of clean GaAs(001)-(2x4) (left) and Ga_2O inserted into the dimers (right). The top line scans run across the As dimer row direction ([110]), and the bottom two line scans are along the rows ([$\bar{1}$10]).

A simple extension of the bonding structure proposed for the low coverage Ga_2O insertion site is used to explain the bonding structure for monolayer coverage of Ga_2O deposited on the GaAs(001)-(2x4) surface at an elevated surface temperature. Fig. 4 shows a filled state STM image of a monolayer of Ga_2O/GaAs(001) taken with a bias of -1.5 V and a tunneling current of 0.2 nA. At monolayer coverage of Ga_2O, the surface has rows that run perpendicular to the original arsenic dimer rows. We find good agreement between the Tersoff-Hamman STM simulations [39] using the plane wave/pseudo-potential DFT code VASP [40], [41] and our proposed monolayer structure [27]. The initial (2x4) surface has an intrinsic arsenic deficiency compared to that of the proposed (2x2) surface structure. The proposed (2x2) surface structure contains a single monolayer of arsenic whereas the initial (2x4) surface only contains 0.75 monolayers of arsenic. It is proposed that the surface reconstructs to form steps as a result of the arsenic deficiency. By taking numerous line scans across the newly formed Ga_2O rows (along the $[\bar{1}10]$ azimuth), a line spacing distribution is obtained as shown in Fig. 5. The graph

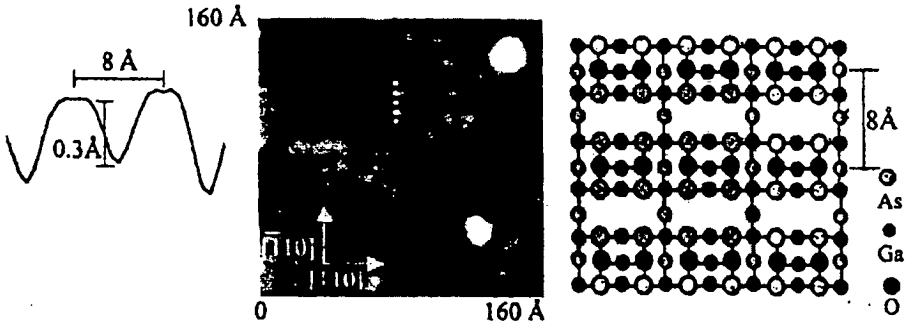

Figure 4. The center filled state STM image of monolayer coverage of Ga_2O adsorbed on the clean GaAs(001)-(2x4) surface at elevated temperature as taken at V = -1.5 V and I = 0.2 nA (center). Line scan analysis (left) taken along the dotted line drawn on the STM image corresponds well to the proposed atomic placement in the ball-and-stick diagram (right).

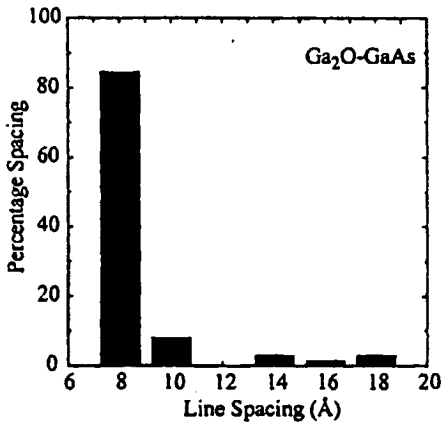

Figure 5. Percentage spacing as a function of consecutive line spacing shows that Ga_2O fully saturates at a line spacing of 8 Å. The near uniform spacing is a result of a surface reconstruction that liberates As to reduce strain.

shows that Ga_2O fully saturates the surface at a line spacing of 8 Å and our STM images at monolayer coverage are very near full saturation. The surface reconstruction allows for the formation of a uniform monolayer.

The electronic structure of the surface at monolayer coverage is studied by STS. The spectroscopic technique holds the tip within a few angstroms from the surface and a bias is swept through the sample while the differential conductivity is measured using a lock-in amplifier. The differential conductivity is then divided by a broadened I/V curve, $(\overline{I/V})$, to arrive at a unit-less quantity which is a good approximation of the density of states in the near surface region. In Fig. 6, the measured STS spectra of monolayer coverage of Ga_2O on both p- and n-type GaAs(001) is shown. Both materials show a bandgap of ~1.5eV, very close to the GaAs bulk value of 1.43 eV [42], [43]. The small discrepancy in the surface bandgap compared with that of bulk GaAs is due to the low doping levels of both materials. The samples were doped with $2x10^{16}$ cm^{-3} Be and $2x10^{16}$ cm^{-3} Si for the p and n-type material, respectively. The density of states and the Fermi level position for both p and n-type material are indicative of unpinned surfaces with no measurable states in the bandgap.

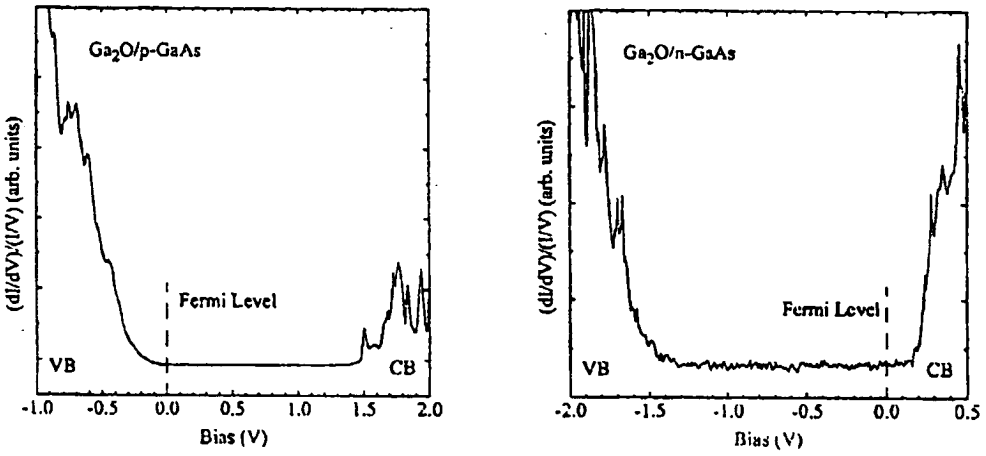

Figure 6. Scanning tunneling spectroscopy spectra of monolayer coverage of Ga_2O adsorbed onto both p- and n-type GaAs(001)-(2x4). The Fermi level position is near the valence band edge and conduction band edge for p and n-type material, respectively.

Density functional theory calculations are performed on the GaAs-β2(2x4) surface to model the energetics of surface reactions, different bonding configurations and corresponding electronic structures. A plane-wave pseudopotential approach is implemented along with the PW91 GGA-DFT method using the VASP code [40], [41]. The clean GaAs-β2(2x4) surface is modeled with an 8-layer slab consisting of 32 gallium and 28 arsenic atoms, terminated with pseudo-hydrogen (H with 1.25 valence electrons to mimic bulk arsenic bonding), and utilizing periodic boundary conditions. All structures shown are allowed to fully relax and are rigorously checked with respect to plane-wave and k-point sampling convergence. Adequate values are determined to be 500 eV plane-wave cut-off with a 4x2x1 Monkhorst-Pack k-point sampling in the 1st Brillouin zone.

Fig. 7 shows two side-on models of the GaAs-β2(2x4) surface. Model (a) shows the clean unit cell. Model (b) shows a Ga_2O molecule inserted into two arsenic dimers (gallium atoms from Ga_2O molecule are marked with an asterisk). Model (c) shows a top-down view of the clean GaAs-β2(2x4) surface. Tersoff-Hamman STM simulations confirm that these are the correct surface structures [27], [39].

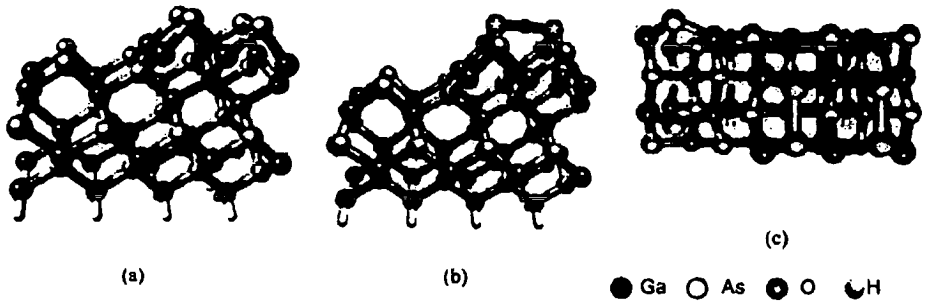

Figure 7. Model (a) shows a side view of a clean GaAs-β2(2x4) surface, (b) shows a side view of the same surface with Ga_2O inserted into the arsenic dimer pair, and (c) shows a top view of the clean surface.

Fig. 8 shows the electronic structure of the bonding model depicted in Fig. 7. The density of states (DOS) is calculated as a function of energy and is shown in the bandgap region for both discussed structures. The solid blue line in Fig. 8 shows the clean GaAs-β2(2x4) surface DOS; it exhibits a band-gap region free of electronic states. The green line in Fig. 8 shows the DOS of the clean GaAs-β2(2x4) surface with a Ga_2O molecule inserted into the arsenic dimer pair. This calculation confirms that the adsorption of Ga_2O onto the clean surface does not induce states within the bandgap. Using the surface Ga_2O monolayer as a template, further oxide deposition proceeds via the formation of Ga_2O_3 with an amorphous microstructure as discussed in the next section.

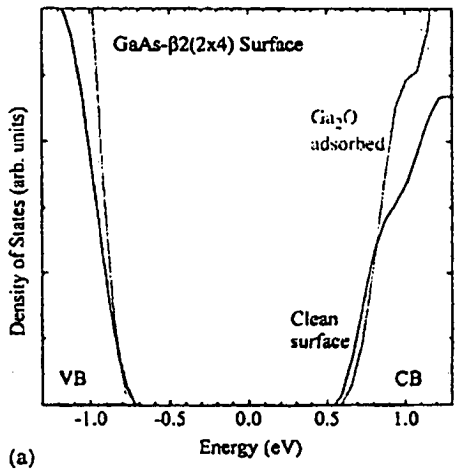

Figure 8. Calculated DOS for both clean and Ga_2O adsorbed surfaces shown in Fig. 7.

3 Deposition technique

An effusive evaporation technique has been developed to deposit Ga_2O_3 thin films on GaAs(001) substrates in a production-type molecular beam epitaxy (MBE) system [26]. A polycrystalline Ga_2O_3 charge heated in a high-temperature effusion cell is used as the evaporation source. In this section, atomic force microscopy (AFM), ellipsometry, electron diffraction, and transmission electron microscopy (TEM) is used to characterize the Ga_2O_3 -GaAs structures. Under optimal deposition conditions, the Ga_2O_3 film surface is atomically smooth as revealed by AFM, while the Ga_2O_3-GaAs interface is atomically abrupt as confirmed by cross-sectional TEM.

Preferentially, Ga_2O_3 deposition runs are carried out in a production-type V100 dual-chamber multiwafer MBE system (VG Semicon). One chamber is dedicated for the growth of GaAs-based III-V semiconductor device structures while the second chamber is configured for oxide deposition. Both chambers are equipped with reflection high energy electron diffraction (RHEED) for in-situ monitoring of the surface during GaAs epilayer growth and during the initial stage of oxide deposition. The base pressure in both chambers is below mid-10^{-10} Torr. For oxide deposition, a polycrystalline Ga_2O_3 charge thermally heated in a high-temperature effusion cell and a rf plasma oxygen source are used for providing the oxide molecular flux and activated oxygen, respectively. An Ir crucible is used in the high-temperature cell. The chamber pressure during oxide deposition typically ranges from about $5x10^{-7}$ Torr to about $7x10^{-6}$ Torr and the oxygen plasma operation power is varied from 350 W to 550 W.

Commercial GaAs(001) substrates up to 6-inch in diameter are employed in this study. GaAs epitaxial layer are grown under standard growth conditions after the thermal desorption of the native oxide in the III-V chamber. A sharp and streaky As-stabilized GaAs(001)-(2x4) RHEED pattern is obtained after the epilayer growth, indicating an atomically ordered and flat GaAs(001) surface. The epitaxial GaAs substrates are either covered by an arsenic cap layer or transferred directly from the III-V chamber to the oxide growth chamber via a UHV buffer chamber. Fig. 9 shows a typical GaAs epitaxial layer structure utilized in this study. After the epitaxial GaAs substrate has been loaded into the oxide chamber, the substrate temperature is ramped up to the deposition temperature in the range of 350-550 °C until a sharp and streaky (2x4) RHEED pattern is obtained. The polycrystalline Ga_2O_3 charge in the high-temperature cell is then heated to its setpoint to produce a molecular oxide flux (see Section 2). A background oxygen in the order of $7x10^{-8}$ Torr is typically observed upon heating from the charge oxide decomposition. Once the substrate and high-temperature cell temperatures reach their equilibrium, the oxide cell and oxygen source shutters are opened such that the

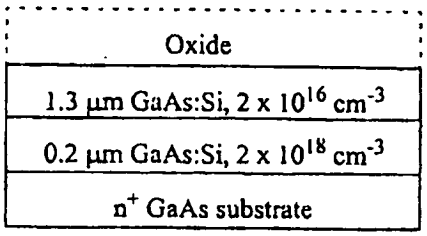

Figure 9. Epitaxial layer structure optimized for photoluminescence (PL) and capacitance-voltage (CV) measurements. The gate oxide to be deposited is indicated by a dashed line.

GaAs-(2x4) surface is exposed to the molecular oxide flux to commence the oxide deposition. Optionally, low levels of additional molecular oxygen can be provided at the initial stage of the oxide deposition and rf plasma activated oxygen for the remainder of the Ga_2O_3 film deposition. In some cases, only background oxygen from Ga_2O_3 sublimation is used throughout the deposition. In general, rf plasma activated oxygen enhances the deposition rate by up to a factor of 3.

The following reactions may occur on the substrate surface during oxide deposition wherein the Gibbs free energy of formation ΔG_f is given at 700 K:

$$Ga_2O_{(s)} + 2O_{(g)} \rightarrow Ga_2O_{3(s)}, \Delta G_f = -245 \text{ kcal/mol, and} \quad (1)$$

$$Ga_2O_{(s)} + O_{2(g)} \rightarrow Ga_2O_{3(s)}, \Delta G_f = -145 \text{ kcal/mol.} \quad (2)$$

Since ΔG_f is a large negative number in both cases, the reaction rates will be determined by the sticking probabilities of atomic and molecular oxygen, respectively. O_2 has a very low sticking probability on oxides since the O_2 bond is strong. The sticking probability is likely to be especially low on a surface that is, for example, already 99% Ga_2O_3 and 1% Ga_2O. The reaction with atomic oxygen is thus favored based on a lower activation barrier and the oxide formation is kinetically and not thermodynamically controlled.

The surface morphology of Ga_2O_3 oxide films has been studied in detail by AFM. A typical root-mean-square (rms) roughness of the order of 1.0-1.5 monolayer (2.5-3.5 Å) is observed for Ga_2O_3 oxide films deposited at substrate temperatures T_s = 440-450 °C. A roughness as small as 1.6 Å is measured on some films. Fig. 10 shows that monolayer

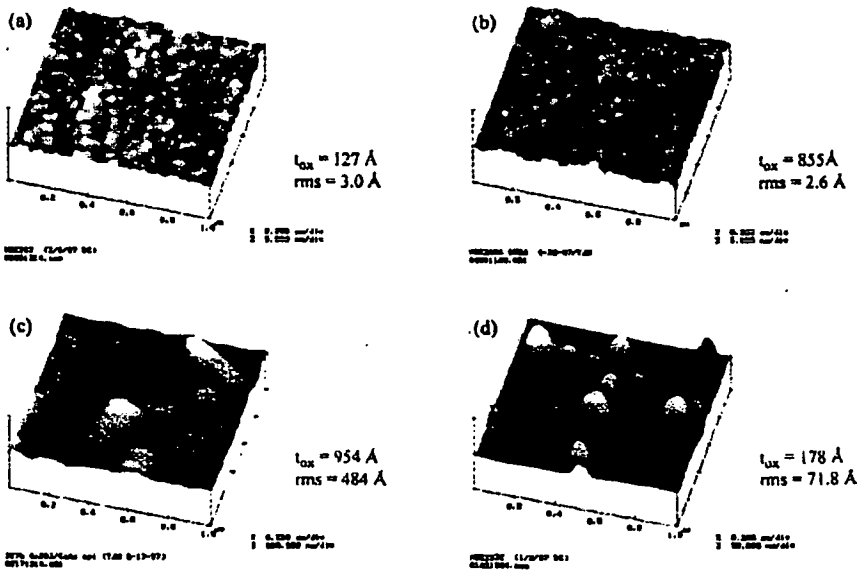

Figure 10. AFM images of a Ga_2O_3 oxide films (a) deposited at T_s = 450 °C using molecular oxygen (4-6x10^{-6} Torr); (b) deposited at T_s = 440 °C using rf plasma activated oxygen (10^{-5} Torr). Plasma power = 400 W; (c) deposited at T_s = 350 °C using rf plasma activated oxygen (10^{-5} Torr). Plasma power = 450 W; (d) deposited at T_s = 500 °C using molecular oxygen (2-3x10^{-5} Torr). The starting GaAs surface had a sharp (4x6) reconstruction.

roughness is obtained when using either molecular O_2 (a) or rf plasma activated oxygen (b). The films are deposited at T_s = 450 °C and 440 °C and their thicknesses are 127 Å and 855 Å, respectively, as measured by ellipsometry at 632.8 nm. In general, no correlation between film thickness and rms roughness is observed. However, the surface roughness rapidly increases for a substrate temperature beyond the range of about 420-450 °C. This is illustrated in Fig. 10 for T_s = 350°C (c) and for T_s = 500°C (d). The onset and extent of surface roughness also depends on the deposition rate and the supply of rf plasma activated oxygen.

It is worthwhile to note that oxide surface morphology and interface quality are strongly correlated. Fig. 11 is a high resolution cross-sectional TEM image of the Ga_2O_3-GaAs interface including a transmission electron diffraction image of the oxide film. It is clearly evident that the interface is atomically flat and the oxide film completely amorphous.This oxide film was deposited at T_s = 420°C. However, beyond the optimal substrate temperature range of T_s = 420-450°C, crystalline oxide growth is observed and the oxide crystallinity extends to the substrate as evident from high resolution cross sectional TEM images (not shown). This crystalline oxide growth is accompanied by high surface roughness and a pinned Fermi level at the Ga_2O_3 –GaAs interface.

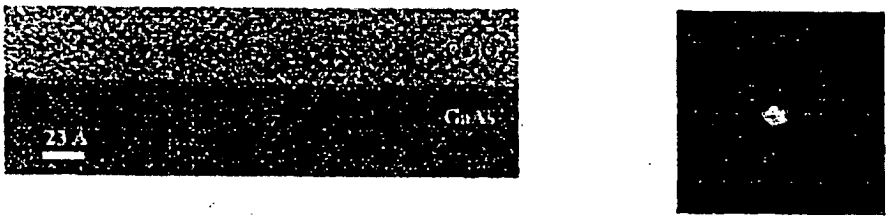

Figure 11. Cross sectional high resolution TEM of a Ga_2O_3-GaAs interface (left) and corresponding electron diffraction pattern of the oxide film (right). This oxide film was deposited at T_s = 420 °C.

4 Film and interface properties

4.1 Structural film properties

Some film properties related to oxide morphology and microstructure have been presented in Section 3 using techniques such as TEM, AFM, and electron diffraction. In this section, further oxide film properties are discussed. Ga_2O_3 films are characterized by Rutherford backscattering (RBS), Auger electron spectroscopy (AES), high resolution x-ray reflectivity, secondary ion mass spectroscopy (SIMS), and ellipsometry. RBS, AES, SIMS, x-ray reflectivity, and ellipsometry provide atomic composition and volume density, atomic composition and depth uniformity, trace impurities, volume density, and film thickness, respectively.

Fig. 12 shows the AES depth profile of a 855 Å thick Ga_2O_3 film deposited at a substrate temperature T_s = 420 °C using polycrystalline Ga_2O_3 as evaporation source and providing additional oxygen flux from a plasma source (wafer MBE305G). The depth uniformity of the oxide film is apparent. The acquired oxygen-to-gallium ratio is compared against a polycrystalline Ga_2O_3 standard. Within the limits of Auger spectroscopy, the oxide films are found to be stoichiometric (60 at.% oxygen, 40 at.% gallium) irrespective of substrate temperature T_s, evaporation source, and supply of

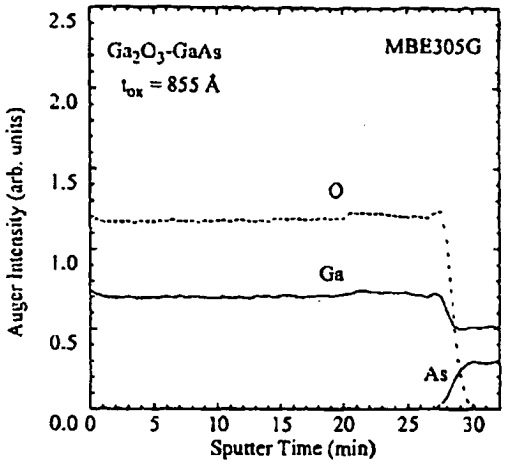

Figure 12. AES depth profile of a 855 Å thick Ga_2O_3 film using polycrystalline Ga_2O_3 as evaporation source and oxygen plasma at T_s = 420 °C.

additional oxygen. This is further discussed in the next paragraph in the context of RBS measurements. Note that e-beam deposited gallium oxide films were only stoichiometric when the substrate was held at room temperature during deposition and additional oxygen was supplied [17]. The standard deviation of oxide thickness is typically less than 1% over a two inch wafer as determined by ellipsometry (not shown).

Fig. 13 shows a RBS spectrum obtained from the oxide film of the same wafer MBE305G. For this film, RBS provides a composition of 62.7 at.% O and 37.3 at.% Ga. Thus, within the limits of RBS, the oxide stoichiometry is confirmed. This is further supported by RBS analysis of 19 oxide films of different thickness and deposited under different conditions: the average oxygen content as determined by RBS is 59.6±1.7 at.%. RBS is further used to measure the volume density ρ of Ga_2O_3 films. Fig. 14 shows the

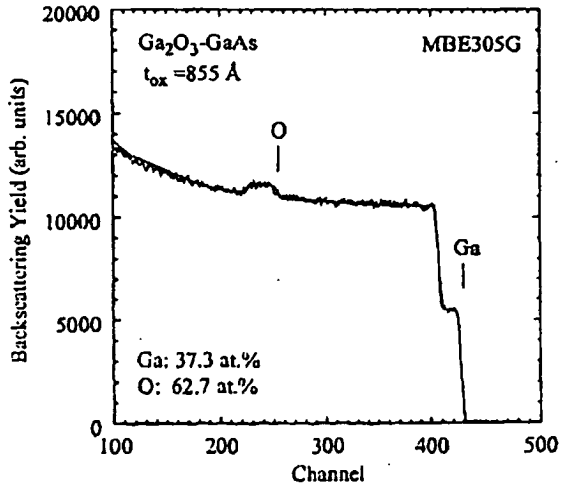

Figure 13. RBS spectrum for a 855 Å thick Ga_2O_3 film using polycrystalline Ga_2O_3 as evaporation source at T_s = 420 °C and oxygen plasma.

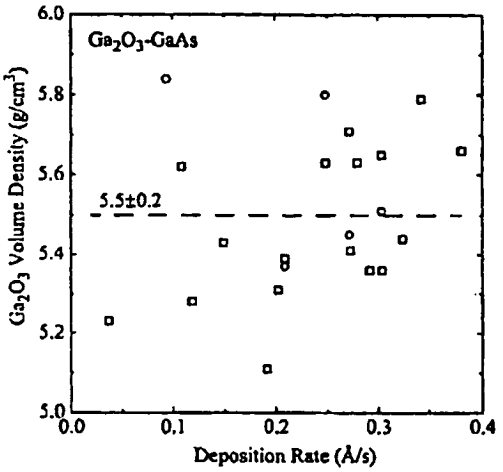

Figure 14. Ga_2O_3 volume density measured by RBS (squares) and x-ray reflectivity (circles) as a function of deposition rate.

volume density as a function of deposition rate. Note that data from both RBS and x-ray reflectivity measurements are shown and that the density appears to be independent of deposition rate: the average density is 5.50 ± 0.20 g/cm^3 as determined from a total of 22 measurement points. This volume density is significantly higher than the volume density of 3.9 - 4.8 g/cm^3 of e-beam deposited gallium oxide films [17]. To our knowledge, no other reports on the volume density of amorphous Ga_2O_3 exist; however, the bulk density of crystalline Ga_2O_3 is well known: 6.4 and 5.9 g/cm^3 for α– and β–Ga_2O_3, respectively [44].

Table 1 shows trace impurities of Ga_2O_3 films deposited on GaAs. The Si, Mg, Al, As, and C concentrations are measured by Quadropole SIMS (PHI Model 6600). The

Table 1. Trace Impurities in Ga_2O_3 films on GaAs. The pressure in the leftmost column reads as follows: Pressure from Ga_2O_3 source only (10^{-6} Torr)/Pressure with additional oxygen from plasma source (10^{-6} Torr).

Sample #	Trace Impurity concentration (cm^{-3})								
	Si	Mg	Al	As	C	La	W	Ta	Mo
98-23, t_{ox} = 188 Å pressure = 1.6	6x10^{18}	1x10^{18}	4x10^{16}	1x10^{19}	6x10^{19}	Oxide film not thick enough for reliable quantification			
98-25, t_{ox} = 640 Å pressure = 1.6/5.4	1x10^{18}	2x10^{17}	1x10^{16}	<1x10^{18}	6x10^{18}	6x10^{16}	< 1x10^{16}	7x10^{17}	6x10^{16}
98-27, t_{ox} = 1140 Å, pressure = 1.1/27	7x10^{17}	1x10^{17}	1x10^{16}	<5x10^{17}	6x10^{18}	6x10^{16}	< 1x10^{16}	6x10^{17}	6x10^{16}
98-34, t_{ox} = 590 Å, pressure= 0.2/21	1.5x10^{18}	1.5x10^{17}	1.5x10^{16}	<3x10^{18}	3x10^{19}	3x10^{16}	not measured		
98-63, t_{ox} = 558 Å, pressure = 1.3/13 + annealing	3x10^{18}	1x10^{17}	8x10^{15}	1x10^{18}	2x10^{19}	4x10^{16}	not measured		

Mo, La, Ta, and W concentrations are acquired by magnetic sector SIMS (Cameca IMS-4f) with the respective detection limits of $1x10^{16}$,$1x10^{16}$, $5x10^{16}$, and $1x10^{16}$. Since Ga_2O_3 SIMS standards were unavailable at the time, SiO_2 SIMS standards are used. Hence, the absolute concentration may be in error by a factor of 2-4, however, the comparisons between samples are accurate to within 5%. The impurity concentrations are typically lower when the film deposition is assisted by an oxygen plasma source. When O plasma is on, the Si, Mg, and Al levels are typically below 10 ppm. Carbon may originate from the chamber background. The As concentration is typically higher for thinner films and is attributed to As release during As cap desorption. The La, W, and Mo impurity concentrations are very low.

4.2 Optical film properties

The oxide thickness t_{ox}, refractive index n, and extinction coefficient k are determined by spectroscopic ellipsometry (SE) over the wavelength range λ from 180 -800 nm. The optical bandgap of the amorphous Ga_2O_3 films is estimated from the dependence of the absorption coefficient on photon energy (Tauc plots).

Fig. 15 shows the refractive index of Ga_2O_3 films with different thickness at λ = 632.8 nm as determined by spectroscopic ellipsometry. The refractive index is 1.896 ± 0.010 and independent of film thickness which indicates an excellent depth uniformity. The refractive index is also not altered when deposition conditions such as substrate temperature T_s, evaporation source, and supply of additional oxygen are varied. Previously, a refractive index n of 1.916 (λ= 632.8 nm) was reported for e-beam deposited Ga_2O_3 [17] and n = 1.92 (no wavelength specified) was given in [44] for crystalline Ga_2O_3. Fig. 16 shows the estimated optical bandgap as a function of chamber pressure. When oxygen is supplied from the Ga_2O_3 source only, an optical bandgap in between 3.1 and 3.8 eV (circles) is measured. In this case, the chamber pressure is $\cong 10^{-6}$ Torr. The supply of additional oxygen raises the chamber pressure and increases the optical bandgap; in particular the use of the oxygen plasma source widens the optical bandgap to as high as 4.7 eV (diamonds and triangles). This is well within previously

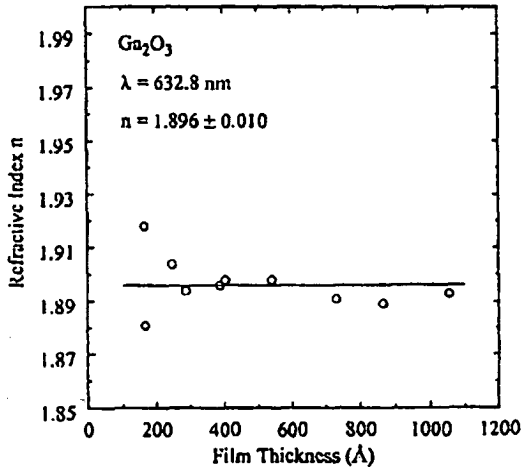

Figure 15. Refractive index of various Ga_2O_3 films at 632.8 nm wavelength as determined by spectroscopic ellipsometry.

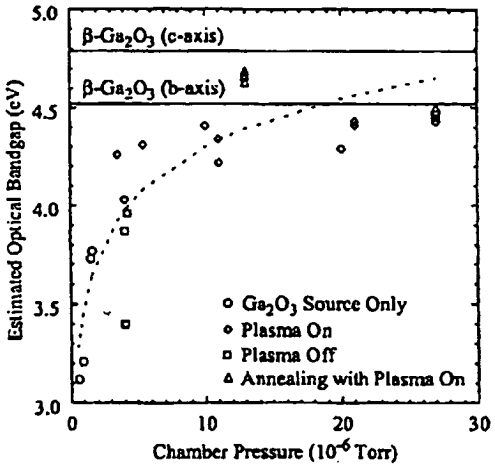

Figure 16. Bandgap of amorphous (symbols) Ga_2O_3 as a function of chamber pressure during deposition. The dashed line is a guide to the eye.

reported bandgaps for crystalline Ga_2O_3; an optical bandgap of 4.52 and 4.79 eV was reported along the b and c axis of single crystal β-Ga_2O_3, respectively [45]. For comparison purposes, the bandgaps of single crystal β-Ga_2O_3 are also shown in Fig. 16.

4.3 Electrical interface and film properties

Electrical film and interface properties are measured using current voltage (I-V),

4.3 Electrical interface and film properties

Electrical film and interface properties are measured using current voltage (I-V), capacitance-voltage (C-V), and photoluminescence intensity (PLI) measurements. All measurements are done at room temperature. The photoluminescence intensity technique enables interface optimization without sample processing and, in combination with standard capacitance-voltage measurements, virtually eliminates common pitfalls in insulator-III-V semiconductor interface characterization. All data discussed in this section are obtained from the test structure shown in Fig. 9. The epitaxial layers of this test structure are optimized for PLI and C-V measurement and analysis. For C-V and I-V measurements, circular metal dots (Ti/Au) with diameters d of 50, 250, and 500 μm are deposited on top of the oxide and a blanket metal deposit (Ge/Ni/Au) is done on the substrate backside.

Fig. 17 shows typical I-V curves obtained from Ga_2O_3-GaAs structures. Large leakage currents are observed for low voltage for both negative and positive polarity. Here, the polarity is defined with respect to the metal dot deposited on top of the oxide. A Ga_2O_3 specific resistivity ρ of the order of 400 - 700 Ω cm is estimated from the slope of the I-V characteristics. At a first glance, these large currents may appear to be inconsistent with the observation of a stoichiometric oxide and an optical bandgap as high as 4.7 eV. However, strong electrical conduction only requires defect densities of the order of 10^{18} cm^{-3} within the oxide bandgap, levels which are far below the detection limit of structural analysis techniques such as RBS and optical techniques such as ellipsometry.

Extensive post-deposition annealing studies were performed to address the issue of high oxide conductivity. Different plasma source designs provided partial pressures of

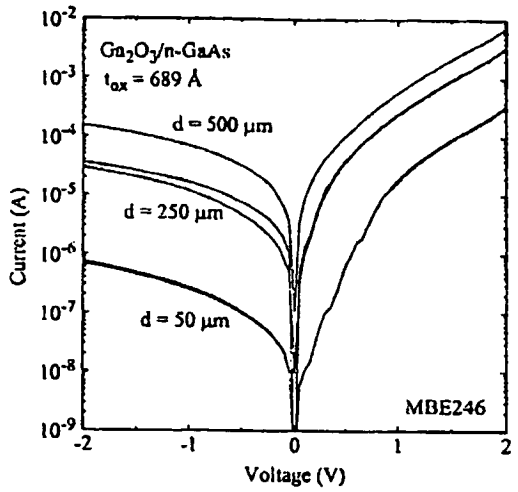

Figure 17. Measured room temperature I-V curves of Ga_2O_3/n-GaAs test samples with different metal dot diameter d. The current scales approximately with area.

active oxygen of about 0.1 - 0.2 Torr (mostly O) and of about 5 Torr (O_3). Samples were treated in a range of substrate temperature from room temperature to 500 °C for periods of 30, 60, and 120 min. The maximum specific resistivity obtained is estimated to 10^4 Ω cm. Thus, electrical Ga_2O_3 bulk properties could only be marginally improved. The lack of response to active oxygen exposure suggests that the defects responsible for conduction are not related to oxygen vacancies or the defect nature of the amorphous network is complex and defects cannot be removed by exposure to active oxygen under the above discussed conditions.

Fig. 18 shows a typical result of a 1 MHz C-V measurement (dashed lines). For comparison purposes, a high frequency (hf) capacitance-voltage simulation is shown

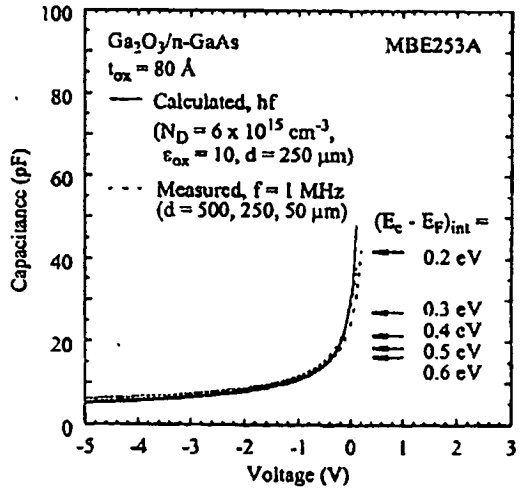

Figure 18. 1 MHz C-V measurements (dashed lines) and high frequency (hf) C-V simulation assuming D_{it} = 0 (solid line).

assuming that the interface state density D_{it} equals zero (solid line). Note that quasistatic C-V curves cannot be acquired due to high leakage current. Dot sizes of 500, 250, and 50 μm diameter are measured. Measured data are normalized to the metal dot diameter of 250 μm used in the simulations. Hysteresis is not observed in the measurement and the calculated curves fit the measured data well. The horizontal lines included in Fig. 18 indicate the distance between the GaAs conduction band edge E_c and the Fermi energy level E_F at the Ga_2O_3-GaAs interface $(E_c\text{-}E_F)_{int}$. Note that C-V measurements fail towards accumulation for $E_F \geq E_c$ -0.2 eV due to excessive leakage currents (positive bias). Further, steady-state deep depletion is observed under negative bias when E_F falls below the intrinsic energy level E_i (E_c - E_i = 0.67 eV for GaAs). Since C-V data do not contain information about interface states D_{it} in steady-state deep depletion [46], the measured C-V data may be applied to D_{it} analysis within the range of $E_i \leq E_F \leq E_c$ - 0.2 eV only. Considering standard techniques for D_{it} analysis such as the quasistatic- high frequency technique (qs/hf) [47] and the Terman method [48], the serious limitations of the acquired data become apparent: The qs/hf method is not applicable since quasistatic data are unavailable and the Terman method fails since the difference between measured and calculated hf C-V curves is below the detection limit of Terman's method. Hence, quantitative interface characterization has been mainly accomplished by a photoluminescence intensity technique as described in the following section.

The photoluminescence intensity technique has been introduced as a standard tool to monitor the interface and surface quality during device fabrication [23]. This technique is based on the radiative intensity I_{PL} of the spontaneous emission (photoluminescence, PL) of a direct-gap semiconductor [49] as a function of incident light density on the sample surface P_0 ($10^{-1} \leq P_0 \leq 10^4$ W/cm^2) wherein the measured steady-state I_{PL}-P_0 dependence is analyzed using an advanced self-consistent drift-diffusion model [46]. The efficacy of the PLI technique strongly depends on the range of excitation power, the laser spot size, and the design of the test structure. Some basics of the experimental and analysis techniques are discussed in the following; the reader is referred to Refs. [29] and [31] for further details.

Fig. 19 shows a block diagram including the essential components of the optical measurement system. Excitation is provided by a Spectra Physics argon ion laser with a nominal maximum power output of 5 watts emitting at λ_0 = 514.5 nm. A first Oriel motorized filter wheel system equipped with one set of Oriel absorptive neutral density filters with optical densities of 1, 2, 3, and 4, and a second Oriel motorized filter wheel system equipped with another set of Oriel absorptive neutral density filters with optical densities of 0.3, 0.5, and 0.8 provide a maximum combined attenuation of 6.9 x 10^4. A telescope comprising two lenses with a focal length of 120 and 80 mm, respectively, is used to adjust the focal plane of the incoming laser beam which enters through the microscope illumination port at the microscope's backside. The microscope is equipped with a customized stage comprising a Newport 406 dual axis translation stage having two DM-13 differential micrometers with 0.07 μm resolution, and a 488 Newport rotary platform with 10 μm vertical resolution. A full-width-at-half-maximum (FWHM) of 35 μm is measured for the laser spot on the sample surface. The collimated luminescence beam emitted from a test sample positioned on the stage of the microscope exits on the microscope's top where a 514.5 nm laser line filter is used to filter out laser light reflected by the test sample's surface. The collimated luminescence beam is attenuated

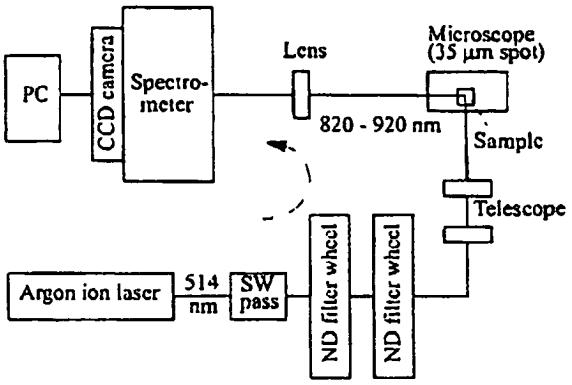

Figure 19. Experimental setup for photoluminescence intensity measurements to characterize oxide/III-V semiconductor interfaces.

as required using Oriel glass metallic neutral density filters with optical densities of 1, 2, 3 and 4 providing a maximum attenuation of 3.97×10^3. Subsequently, the PL signal is coupled into a spectrometer manufactured by Acton Research Corporation using various mirrors and a lens with a focal length of 100 mm. Finally, the PL spectra are acquired by a model ST-6 CCD camera.

Fig. 20 shows measured normalized PL spectra for selected test structures at various excitation densities $P_0' = TP_0$ where P_0' and T are the light density entering the semiconductor surface and the optical transmissivity of the sample surface at the excitation wavelength λ_0, respectively. Starting at the highest curve for each test structure, $P_0' = 6.6\text{x}10^3$, $7.1\text{x}10^1$, $5.6\text{x}10^{-1}$ W/cm^2 for hydrogen passivated Ga_2O_3-GaAs, $6.9\text{x}10^3$, $7.4\text{x}10^1$, $5.8\text{x}10^{-1}$ W/cm^2 for as-deposited Ga_2O_3-GaAs, and $6.5\text{x}10^3$, $5.5\text{x}10^{-1}$ W/cm^2 for the bare surface, respectively. The spectra shown in Fig. 20 are normalized to

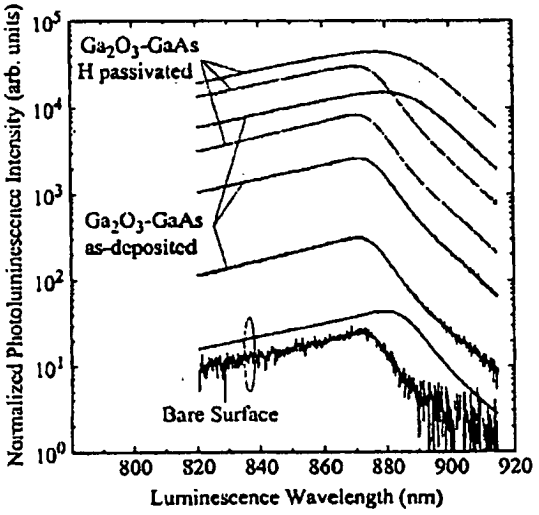

Figure 20. Selected normalized measured PL spectra of Ga_2O_3-GaAs interfaces and bare GaAs substrate with the light density P_0' as a parameter (see text for further details).

the excitation density P_0' and the optical transmissivity of the sample surface at the PL wavelength of 870 nm is also taken into account. The Ga_2O_3 film thickness is 74 Å. We will discuss next some basics of our modeling approach.

A calculated energy-band diagram of the investigated structure (see Fig. 9) is depicted in Fig. 21 for an excitation density P_0' of 0.1 W/cm^2 (λ_0 = 514.5 nm) entering the semiconductor surface. The band diagram is calculated based on an extended self-consistent drift-diffusion model [46] including defect-mediated Shockley-Read-Hall recombination occurring at interfaces via a continuum of interface states D_{it} (r_{SRH}) [49] and due to trapping centers of density N_t located at discrete energy levels E_t [50] in the semiconductor bulk (R_{SRH}). Here, E_v, E_{Fn}, E_{Fp}, S_n, S_p, σ_n, σ_p, h, and ν are the valence band edge, the quasi Fermi level for electrons and holes, the interface recombination velocity for electrons and holes, the capture cross section for electrons and holes, Planck's constant, and the photon frequency of the incident light, respectively.

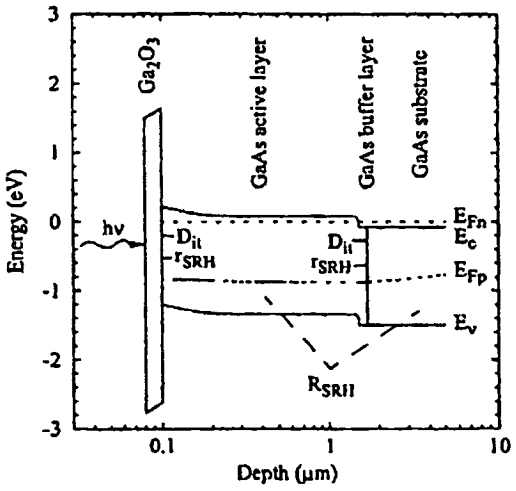

Figure 21 Calculated energy-band diagram of the investigated Ga_2O_3-GaAs structure. The active layer (1.4 μm) and the buffer layer (0.2 μm) were grown on GaAs substrate by molecular beam epitaxy. The energy-band diagram is calculated using the following oxide-GaAs interface parameters: D_{it} = 1.6 x 10^{11} cm^{-2} eV^{-1}, $\sigma_n = \sigma_p$ = 2.2 x 10^{-14} cm^2, and $S_n = S_p$ = 3.2 x 10^4 cm/s. The energy is shown relative to the bulk Fermi level in equilibrium.

The test structure shown in Fig. 9 is optimized such that the PL signal I_{PL} is emitted primarily from a lightly doped n-type (donor concentration N_D = 2 x 10^{16} cm^{-3}) GaAs active layer (see Fig. 22). This is accomplished by inserting a highly doped GaAs buffer layer (N_D = 2 x 10^{18} cm^{-3}) between the GaAs substrate ($N_D \cong$ 2 x 10^{18} cm^{-3}) and the lightly doped active layer. As demonstrated in Ref. [29] and [46], the only resulting unknown parameters which effectively determine I_{PL} in such a test structure are the state density D_{it} and the capture cross sections σ at the interface or surface to be investigated.

Fig. 23 shows measured (symbols) and calculated (lines) internal quantum efficiencies η as a function of excitation power density P_0' for as-deposited Ga_2O_3-GaAs structures (triangles), hydrogen plasma exposed Ga_2O_3-GaAs structures indicated by diamonds (further discussed below) and baseline samples (circles and squares). The

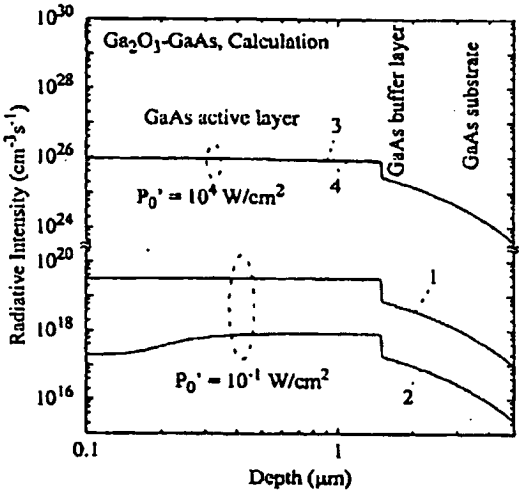

Figure 22. Calculated depth profiles of the radiative GaAs emission (PL) of the investigated Ga_2O_3-GaAs structure. The following oxide-GaAs interface parameters are used: $S_n = S_p = 3.2 \times 10^4$ cm/s and $D_{it} = 0$ (curve 1 and 3) and $D_{it} = 1.6 \times 10^{11}$ cm^{-2} eV^{-1} (curve 2 and 4). 88.6%, 87.5%, 84.0%, and 83.9% of the total spontaneous emission originates from the active layer for curve 1, 2, 3, and 4, respectively.

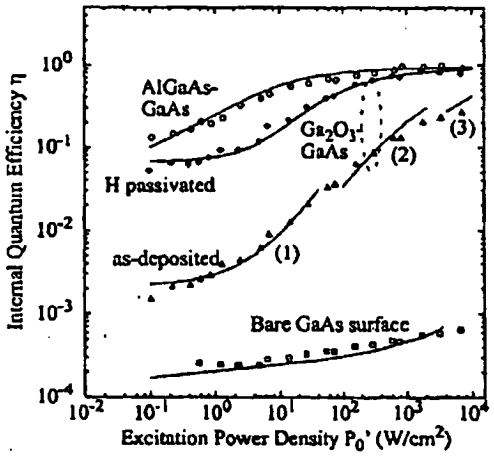

Figure 23. Measured (symbols) and calculated (lines) internal quantum efficiencies η as a function of excitation power density P_0'. The excitation wavelength is 514.5 nm. $S_n = 2\text{x}10^4$, $3.2\text{x}10^4$, and $5\text{x}10^4$ cm/s for curves labeled (1), (2), and (3), respectively.

experimental results have been obtained as follows: Measured PL intensities I_{PL} are attained by integrating the normalized GaAs PL spectra from 820 to 910 nm wavelength (Fig. 20) for each excitation power density P_0'; the thus acquired I_{PL}/I_0' curves are shifted along the vertical η axis to the position of the calculated curves obtained from integrating the depth profile of radiative intensity (Fig. 22) using one normalization factor for all measured curves. Here, $I_0' = P_0' / h\nu$ where ν is the photon frequency of the incident light. In order to unequivocally map the measured characteristics onto the

calculated curves, a range for P_0' of five orders of magnitude including very high injection ($P_0' \geq 10^3$ W/cm^2), high injection (10^3 W/cm^2 > $P_0' \geq 10$ W/cm^2), and low injection ($P_0' < 10$ W/cm^2) is required, and both baseline structures with low D_{it} ($\eta \cong 1$, AlGaAs-GaAs interface) and very high D_{it} ($\eta \cong 0$, bare GaAs surface) must be provided. Before we summarize the interface properties, we discuss hydrogen plasma exposure of the as-deposited Ga_2O_3 -GaAs interface structure in the following.

In striking analogy to the SiO_2-Si, system, hydrogen atoms are found to passivate defects at as-deposited Ga_2O_3-GaAs interfaces [30] as indicated by the significant improvement of quantum efficiency after hydrogen exposure (Fig. 23). Hydrogen exposure of as-deposited Ga_2O_3-GaAs structures with varying oxide thickness is conducted in a Tegal 6000 etching tool where the atomic hydrogen is provided by an RF plasma discharge device with a frequency of 13.56 MHz. The following parameter range is explored: RF power 5 - 500 W, pressure 2 - 75 mTorr, hydrogen flow 10 sccm, and exposure time 5 - 300 s. The efficiency of interface passivation is found to depend only slightly on plasma parameters; however, no interface passivation could be observed when the RF source was turned off. The substrate is not intentionally heated but we estimate that the sample surface temperature reaches up to about 150 °C during plasma treatment.

The quantum efficiency data shown in Fig. 23 are correlated to the presence or absence of hydrogen at the Ga_2O_3-GaAs interface as determined by SIMS. Fig. 24 shows the corresponding hydrogen concentration depth profiles of the above discussed Ga_2O_3-GaAs structure with a 74 Å thin Ga_2O_3 layer as-deposited (circles) and after hydrogen plasma exposure (diamonds) as measured by SIMS. Conversion of ion counts to concentrations was accomplished by using relative sensitivity factors derived from ion-implanted Ga_2O_3 standards which were analyzed along with our test samples. Whereas the interfacial hydrogen signal is at or below the detection limit of the instrumentation ($\cong 5 \times 10^{18}$ cm^{-3}) for the as-deposited structure, a clear shoulder with an interfacial hydrogen concentration above 10^{20} cm^{-3} is observed after hydrogen plasma exposure.

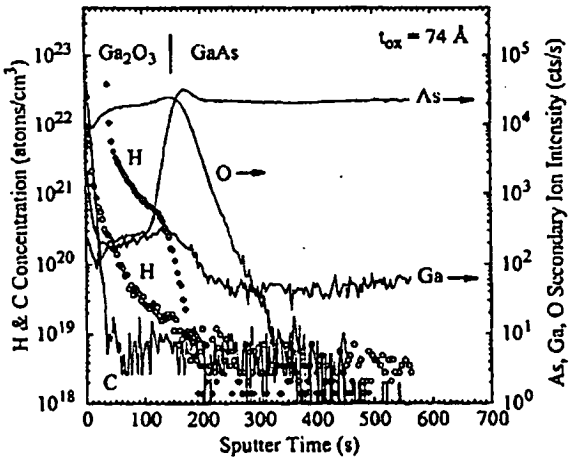

Figure 24. Concentration (H, C) and secondary ion intensity (As, Ga, O) depth profiles of the Ga_2O_3-GaAs structure as measured by SIMS. The hydrogen concentration profiles are shown before (circles) and after (diamonds) hydrogen plasma exposure.

The increase of hydrogen and carbon concentration towards the surface for both as-deposited and hydrogen plasma exposed samples is due to surface hydrocarbons. Table 2 summarizes Ga_2O_3-GaAs, AlGaAs-GaAs interface and GaAs surface properties. The electrical interface parameters in Table 2 comprise the parameter set used to obtain the best fit (lines) to the measured data (symbols) in Fig. 23; the interface hydrogen concentration is taken from the SIMS data shown in Fig. 24.

Table 2. Ga_2O_3-GaAs, AlGaAs-GaAs interface and GaAs surface properties.

Structure	Interface State Density D_{it} ($cm^{-2}eV^{-1}$)	Capture Cross Section σ (cm^2)	Interface Recombination Velocity S (cm/s)	Interface Hydrogen Concentration (cm^{-3})
Ga_2O_3-GaAs H plasma	$\leq 3.5 \times 10^{10}$	9.7×10^{-15}	4×10^3	$> 10^{20}$
Ga_2O_3-GaAs as-deposited	10^{11} (midgap) $\geq 10^{12}$ (close to E_c, E_v)	2.0×10^{-14}	2×10^4 (low injection) 5×10^4 (very high inj.)	below detection limit ($\cong 5 \times 10^{18}$)
AlGaAs-GaAs	not determined		1.2×10^3	not applicable
GaAs Surface	$> 10^{13}$	5×10^{-14}	10^7	not applicable

4.4 Thermal stability

In this section, we investigate the correlation between structural and electrical properties at the Ga_2O_3-GaAs interface under thermal stress and we determine the mechanism of interface destruction which occurs above a critical temperature T_c. As outlined in Section 3, as-deposited Ga_2O_3 films are found to be amorphous forming an atomically abrupt interface of low interface state density D_{it} with GaAs. Rapid thermal annealing (RTA) above a critical temperature T_c = 720 °C induces Ga_2O_3 bulk crystallization, resulting in structural deformation of the Ga_2O_3-GaAs interface and complete destruction of its low D_{it} character for thicker oxide films ($t_{ox} \geq 127$ Å). Further, preliminary data suggest that the critical temperature T_c may increase in the limit of very thin Ga_2O_3 films.

Prior to RTA, the Ga_2O_3-GaAs structures are capped by a silicon nitride layer using a standard chemical vapor deposition technique. Thermal annealing is done in a standard RTA tool by subjecting test samples to a target temperature in between 300 and 800 °C for 6 s in nitrogen gas. Subsequent to RTA, the silicon nitride film is removed using a dry etch process. Cross sectional transmission electron microscopy images, electron diffraction patterns, and PL intensity data are acquired and analyzed before and after RTA.

Fig. 25 shows high resolution cross sectional TEM micrographs of (a) a 700 °C and (b) a 780 °C rapid thermal annealed Ga_2O_3-GaAs test sample. The TEM micrograph of the as-deposited film is shown in Fig. 11. The oxide thickness for all three samples is 689 Å. The interface is atomically abrupt for the as-deposited and 700 °C annealed test sample. However, crystallinity is observed in the oxide and structural deformation

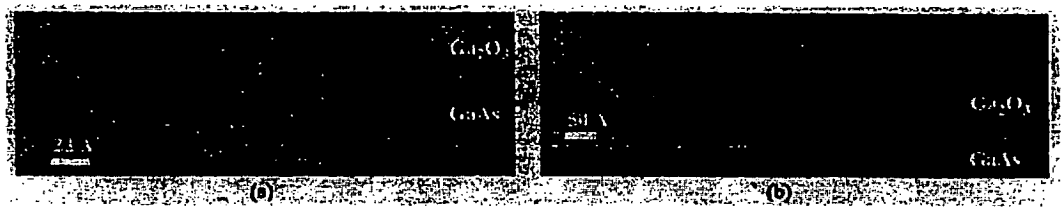

Figure 25. High resolution cross sectional TEM micrographs of (a) a 700 °C and (b) a 780 °C rapid thermal annealed Ga_2O_3-GaAs test sample. Note the crystallinity in the oxide and the interface deformation in (b).

occurs at the Ga_2O_3-GaAs interface after RTA at 780 °C (Fig. 25b). Crystalline "hillock" type spots with a typical lateral size and spacing of 70 - 100 Å form in some areas at the Ga_2O_3-GaAs interface. The light and dark contrast in the oxide show oxide grains of different orientation. The dark grains are oriented close to a diffraction condition and the lighter grains are not close to a diffraction condition. Fig. 26 shows the corresponding electron diffraction patterns after (a) RTA at 700 °C and (b) RTA at 780 °C. Again, the electron diffraction pattern for the as-deposited Ga_2O_3 film is shown earlier (Fig. 11). The diffraction patterns in Fig. 26 also include the (110) single crystal diffraction pattern from the GaAs substrate. For the as-deposited and 700 °C annealed films, a diffuse halo surrounded by weak halos with rapidly decreasing intensity is indicative of an amorphous oxide microstructure. However, the broad amorphous ring disappears after 780 °C RTA and additional spots are observed originating from the polycrystalline oxide (Fig. 26b). Clearly, oxide crystallinity is thermally induced by annealing at 780 °C.

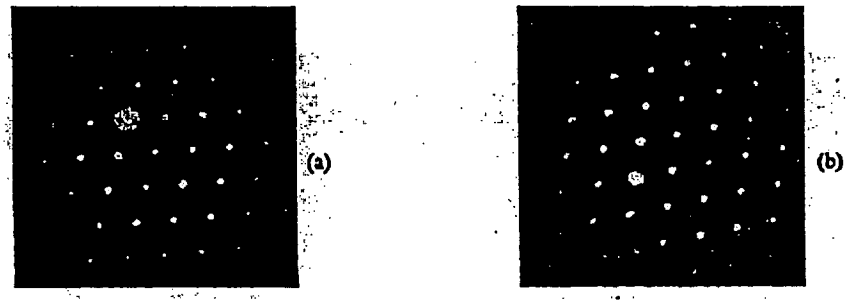

Figure 26. Corresponding electron diffraction patterns after (a) RTA at 700 ° C and (b) RTA at 780 °C. The diffraction patterns also include the substrate which is near the (110) zone. The additional spots in (b) are due to the polycrystalline oxide.

Fig. 27 shows the normalized PL intensity of Ga_2O_3-GaAs test samples as a function of RTA temperature from 300 to 780 °C. Normalization is done in reference to the corresponding as-deposited samples. Data are shown for a large range of Ga_2O_3 film thickness from 78 - 727 Å. A normalized PL intensity around one indicates an electrically intact interface with low recombination velocity S of the order of 2×10^4 cm/s in low injection (compare to Table 2). In contrast, a normalized PL intensity approaching zero characterizes an electrically destroyed interface with an interface recombination velocity exceeding 10^7 cm/s. PL intensities measured for electrically destroyed interfaces are typically lower by a factor of 400 (see also Fig. 23). As shown

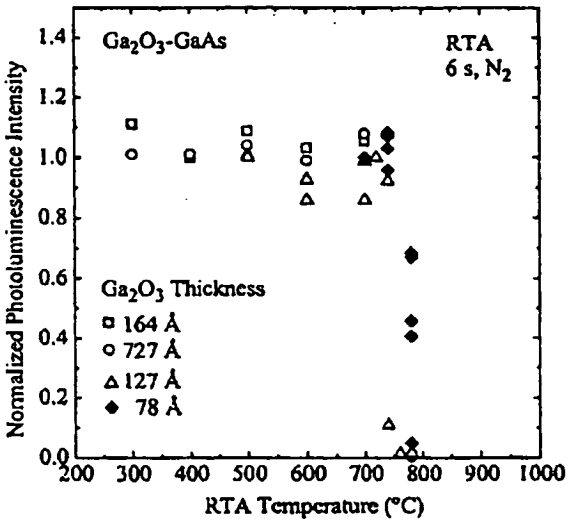

Figure 27. Normalized PL intensity of Ga_2O_3-GaAs test samples as a function of RTA temperature from 300 to 780 °C. Note that the data point for t_{ox} = 164 Å and RTA temperature of 780 °C (open square) is hidden behind the other data points for t_{ox} = 727 Å and 127 Å and RTA temperature of 780 °C (open circle and open triangle).

in Fig. 27, low S interfaces are preserved for RTA temperatures ≤ 720 °C for all Ga_2O_3 thicknesses considered in this study. Therefore, we define here the temperature of 720 °C as the critical temperature T_c. Note that with the exception of the thinnest Ga_2O_3 film (78 Å), all Ga_2O_3-GaAs interfaces are electrically destroyed after RTA at 780 °C. This electrical interface destruction coincides with the appearance of crystallinity in the Ga_2O_3 bulk film and structural deformation of the Ga_2O_3-GaAs interface as evident in the cross sectional TEM micrograph of Fig. 25(b) and the diffraction pattern of Fig. 26(b). Further, the data shown in Fig. 27 for the thinnest oxide film with t_{ox} =78 Å (filled diamonds) indicate that some interface degradation but no complete interface destruction has yet occurred for the thinnest film investigated in this study. This provides preliminary evidence that the critical temperature T_c may increase with decreasing film thickness in the limit of very thin Ga_2O_3 films.

5 Field effect transistor applications

Self-aligned GaAs enhancement mode metal-oxide-semiconductor (MOS) heterostructure FETs (HFET) employing a Ga_2O_3 gate oxide have been successfully manufactured. We chose to use the term *enhancement-mode* rather than *inversion-* or *accumulation-type* since the latter terms become meaningless in the strict sense of inverting a surface from one conduction type to the other or accumulating majority carriers at the surface when semi-insulating substrates and undoped epitaxial layers are used. The p-channel devices with a gate length of 0.6 μm exhibit a maximum dc transconductance g_m of 51 mS/mm which is an improvement of more than two orders of magnitude over previously reported results. With the demonstration of a complete process flow and 66% of theoretical performance, GaAs MOS technology has moved into the realm of reality.

Fig. 28 shows the cross section of a self-aligned p-channel enhancement mode MOS-HFET. The epitaxial layer structure is grown by molecular beam epitaxy on 3" semi-insulating GaAs substrates and consists of a 0.2 μm undoped GaAs buffer layer, a 15 nm undoped $In_{0.2}Ga_{0.8}As$ channel layer, a 15 nm undoped $Al_{0.75}Ga_{0.25}As$ barrier layer, and a 2 monolayer thick GaAs cap layer. A silicon δ-doping with an areal density of $3.3x10^{11}$ cm^{-2} is positioned 3 nm below the channel. The epitaxial layer structure is derived from Motorola's standard CGaAs™ technology [51]. Subsequent to completion of epitaxial layer growth, the wafer platen is transferred under ultrahigh vacuum to a second oxide deposition chamber. Finally, the 9 nm thick Ga_2O_3 gate oxide layer is deposited by thermal evaporation of Ga_2O_3 from an effusion cell. Fig. 29 shows a high resolution TEM cross-sectional micrograph of the completed device layer structure including the electron diffraction pattern of the oxide film. As evident from Fig. 29, the interface between the single crystal semiconductor surface and the amorphous Ga_2O_3 layer is atomically abrupt.

Device fabrication is again built on Motorola's standard CGaAs™ process [51]. A refractory gate metal (TiWN) is used with a 20 nm W diffusion barrier. The source/drain

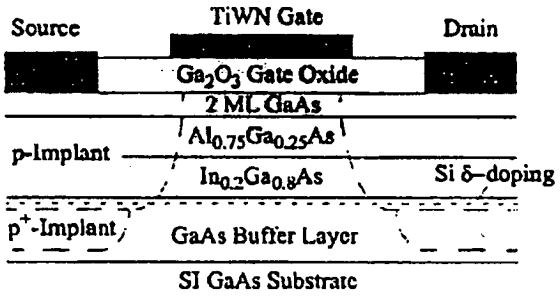

Figure 28. Cross section of a p-channel self-aligned GaAs enhancement mode MOS heterostructure field effect transistors.

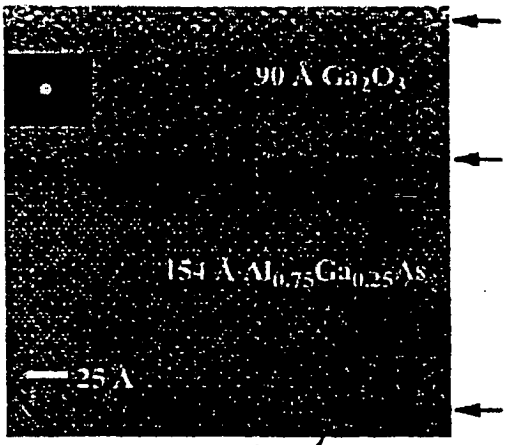

Figure 29. High resolution TEM cross-sectional micrograph of the completed device layer structure. The inset shows the electron diffraction pattern of the oxide film.

implants are implemented self-aligned to the gate and activated by RTA at 700 °C for 10 sec. The implant sheet resistance ρ_s = 1234 Ω/sq. and the contact resistance R_c = 1.05 Ω mm were determined using a transmission line model (TLM). The device dimensions L_G (gate length), L_{GS} (gate-source-spacing), and L_{GD} (gate-drain-spacing) are 0.6 μm, 1.2 μm, and 1.2 μm, respectively.

Fig. 30 shows the measured dc output characteristics of the fabricated 0.6 μm GaAs p-channel MOS-HFET. The transistor characteristics have been measured using a HP4145 semiconductor parameter analyzer; repeated curve scanning has always exactly reproduced the previously measured data. Simulated data (not shown) have been obtained using the two-dimensional simulator PISCES [52] under the assumption of D_{it} = 0. The parameters of the steady-state field velocity relationship have been calibrated based on Motorola's established CGaAs™ technology [53]. The measured and simulated maximum dc transconductance g_m and threshold voltage V_{th} are 51 and 77 mS/mm, and - 0.93 V and - 0.76 V, respectively. Although reduced g_m and shifted V_{th} indicate that interface states still affect the devices to a certain extent, the demonstrated performance of 66% of theoretical dc transconductance is a clear breakthrough. The device uniformity across a 3" wafer is g_m = 46.7 ± 3.9 mS/mm and V_{th} = -0.93 ± 0.1 V.

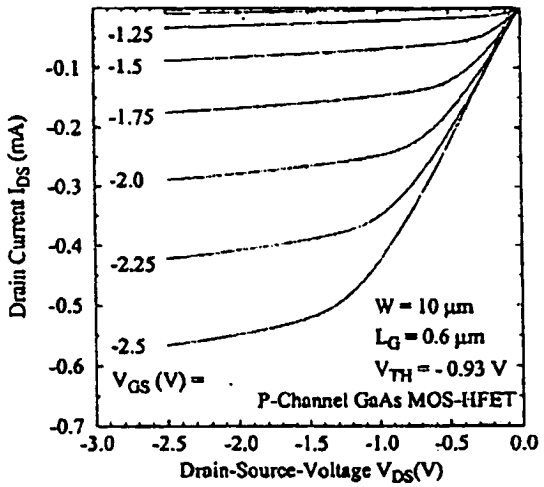

Figure 30. Measured dc output characteristics of a 0.6 μm GaAs p-channel MOS-HFET.

Fig. 31 shows a comparison of published dc transconductance data of enhancement mode GaAs MOSFETs. The comparison to previously reported data will be restricted to enhancement mode FETs which are defined by a threshold voltage $V_{th} > 0$ (n-channel) and $V_{th} < 0$ (p-channel) for the following reasons: (1) enhancement mode is technologically the most important device type and (2), the operation of depletion mode devices does not necessarily require Fermi level unpinning and thus, is not a conclusive indicator of interface quality [46]. For p-channel devices, the highest dc g_m previously reported was 0.3 mS/mm. The dc g_m of our MOS-HFETs is higher by a factor of 170. All previously reported dc g_m data for both n- and p-channel GaAs enhancement mode MOSFETs were at least two orders of magnitude lower than those of competing GaAs technologies such as PHEMT and CGaAs™. A further comparison of previously

published data for GaAs n-channel enhancement mode MOSFETs reveals that essentially no progress had been made since 1978 when a dc g_m of 3.3 mS/mm was reported for a 2 μm GaAs MOSFET.

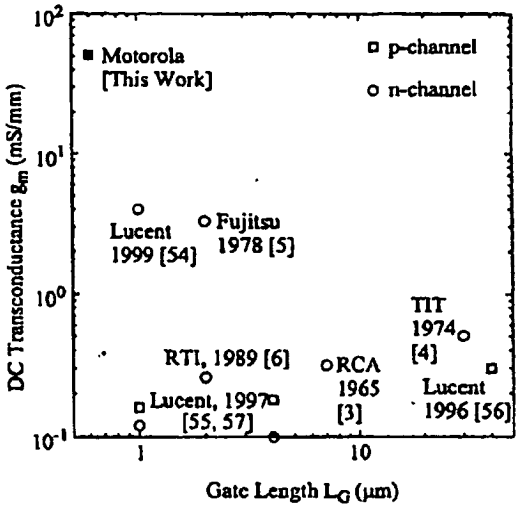

Figure 31. Comparison of dc transconductance data of p-channel (squares) and n-channel (circles) enhancement mode GaAs MOSFETs.

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GALLIUM ARSENIDE MOS TRANSISTORS*

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Abstract—The feasibility of using gallium arsenide for an insulated-gate field-effect (MOS) transistor was investigated. A fabrication process for *n*-channel depletion-type units was developed, and devices were constructed using a simple experimental geometry which had a channel length of 7 μ and a width of 126 μ. The source and drain regions were formed by a planar diffusion of tin; pyrolytically deposited silicon dioxide was used as a mask. The channel region was formed by a special diffusion technique developed for low surface-concentration *n*-type diffusions. Silicon dioxide was used as the gate insulation.

The channel saturation current, which ranged between 50 μA and 25 mA, could be modulated by biasing either the gate or the substrate. The low-frequency (120 c/s) gate transconductance varied up to 700 μ mhos. This parameter was measured as a function of frequency up to 5 Mc and was found to increase with frequency. Substrate transconductances as high as 4000 μ mhos were measured. Analysis of the device characteristics indicated an effective channel mobility of approximately 600 cm^2/V-sec and an interface state density of the order of 10^{12} states/cm^2. The increase in gate transconductance with frequency within the measured range was attributed to interface states having response times between 0·1 sec and 1 μsec.

The effect of fast states on the device characteristics was investigated by use of a model similar to that proposed by SHOCKLEY for junction field-effect transistors.

Résumé—La possibilité d'employer l'arséniure de gallium pour un transistor à déclencheur isolé et effet de champ (MOS) a été examinée. Un procédé de fabrication de dispositifs à type d'épuisement de *n* canaux a été développé et des dispositifs ont été construits en employant une forme géométrique expérimentale simple ayant une longueur de canal de 7 μ et une largeur de 126 μ. Les régions de source et d'épuisement étaient précédemment formées par une diffusion plane d'étain; un masque était formé par la déposition de bioxide de silicium effectuée pyrolytiquement. La région de canal a été formée par une technique de diffusion spéciale développée pour des diffusions de type *n* à faible concentration de surface. Le bioxide de silicium a été employé pour isoler le déclencheur.

Le courant de saturation de canal qui se situe entre 50 μA et 25 mA pouvait être modulé en polarisant soit le declencheur soit la couche inférieure. La transconductance du déclencheur à basse fréquence (120 Hz) a été variée jusqu'a 700 μmhos. Ce paramètre a été mesuré en fonction de la fréquence jusqu'a 5 MHz et on a trouvé qu'il augmente en fonction de la fréquence. Des transconductances de couches inférieures aussi élevées que 4000 μmhos ont été mesurées. Une analyse des caractéristiques du dispositif indique une mobilité de canal effective d'environ 600 cm^2/V-sec et une densité d'état d'interface de l'ordre de 10^{12} états/cm^2. L'augmentation de la transconductance du déclencheur en fonction de la fréquence dans la gamme mesurée a été attribuée aux états d'interface qui avaient des temps de réponse allant de 0,1 sec à 1 μ sec.

Les effets des états rapides sur les caractéristiques du dispositif ont été examinées en employant un modèle similaire à celui proposé par SHOCKLEY pour les transistors à effet de champ.

Zusammenfassung—Es wurde die Möglichkeit untersucht, Galliumarsenid für einen Feldeffekt-Transistor mit isolierter Steuerelektrode (MOS-Transistor) zu verwenden. Ein Herstellungsprozess für Bauelemente vom Trägerverarmungstyp und mit *n*-leitendem Kanal wurde entwickelt, und es wurden Bauelemente hergestellt, die eine einfache experimentelle Geometrie mit einer Kanallänge von 7 μ und eine Kanalbreite von 126 μ hatten. Die Gebiete von Anode und Kathode wurden durch Planar-Eindiffusion von Zinn gebildet; dabei wurde pyrolytisch abgelagertes Siliziumdioxyd als Diffusionsmaske verwendet. Das Kanalgebiet wurde durch eine spezielle Diffusionstechnik

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ATTACHMENT 6

hergestellt, die für Eindiffusion von n-leitendem Material bei niedrigen Oberflächenkonzentrationen entwickelt wurde. Zur Isolierung der Steuerelektrode wurde Siliziumdioxyd verwendet.

Der Kanal-Sättigungsstrom, der zwischen 50 μA und 25 mA lag, konnte durch Vorspannung der Steuerelektrode oder des Unterlagematerials moduliert werden. Die Steilheit bezüglich der Steuerelektrode hatte bei Niederfrequenz (120 Hz) Werte bis zu 700 μA/V. Dieser Parameter wurde als Funktion der Frequenz bis zu 5 MHz gemessen und nahm mit der Frequenz zu. Steilheiten bezüglich des Unterlagematerials bis herauf zu 4000 μA/V wurden gemessen. Eine Analyse der Kennlinien ergab eine effektive Kanal-Beweglichkeit von annähernd 600 cm^2/V-sec und eine Dichte von Störstellen in der Grenzschicht in der Grössenordnung 10^{12} cm^{-2}. Die Zunahme der Steuerelektroden-Steilheit mit der Frequenz innerhalb des gemessenen Bereiches wurde Grenzschicht-Zuständen mit Relaxationszeiten zwischen 0,1 sec und 1 μsec zugeschrieben. Die Auswirkung von schnellen Zuständen auf die Kennlinien wurde mit einem ähnlichen Modell untersucht, wie es SHOCKLEY für Feldeffekttransistoren mit einem p–n Übergang vorschlug.

NOTATION

a	effective channel cross-section
A	$qN_0/2\epsilon$
C_{0x}	oxide capacitance (ϵ_{0x}/t_{0x})
D	channel depth
E_x	electric field in channel, parallel to surface
g_0	zero-bias conductance
g_m	gate transconductance
g_{ms}	substrate transconductance
I_d	source-to-drain current
I_{d0}	source-to-drain saturation current
K	uniform interface state density (per cm^2/V)
L	channel length
m	$C_{0x}(C_{0x}+qK)^{-1}$
N_0	channel concentration
P_0	substrate concentration
q	electronic charge
Q_{st}	total charge in semiconductor space-charge region
Q_{sst}	total charge in interface states
Q_0	total charge in interface states at level band condition
t	ϵ/C_{0x}
t_{0x}	oxide thickness
u	depth of channel depletion from substrate
u_0	depth of channel depletion from substrate when $V_S = 0$
u_s	depth of channel depletion from substrate at drain at saturation
v	depth of channel depletion from interface
v_0	depth of channel depletion from interface when $V_g = 0$
$V_{(x)}$	voltage in channel with respect to source
V_d	voltage at drain
V_{d0}	voltage at drain at saturation
V_g	voltage at gate
V_0	$(Q_0/C_{0x})+\psi_{s0}$
V_{0x}	voltage drop across oxide
V_s	voltage at substrate
W	channel width
ϵ	permitivity of gallium arsenide
ϵ_{0x}	permitivity of oxide
ϕ	built-in potential at substrate-channel junction
ψ_s	interface voltage
ψ_{s0}	interface voltage when $V_g = 0$
σ	conductivity of channel
μ_{avg}	average mobility of channel carriers

INTRODUCTION

THE WORK described in this paper was undertaken to determine the feasibility of using gallium arsenide for metal-oxide semiconductor (MOS) transistors.[1] Figure 1 shows the four types of MOS structures considered. The operating principle of these devices is the control of the source-to-drain conductivity by a transverse electric field which is developed by a voltage applied to the gate. In enhancement-type MOS devices, the source and drain are isolated, and the field is used to invert the surface of the substrate so that a conducting path or channel is formed between the two regions. Depletion-type MOS transistors have an actual channel region whose conductivity may be modulated by the gate field. In this investigation n-channel units were used because device performance is directly related to the mobility of the channel carriers. Because of its high electron mobility, gallium arsenide is an attractive semiconductor material for high-frequency MOS transistors.

The enhancement structure was studied first. Devices were fabricated in which pyrolytically deposited silicon dioxide formed the gate insulation and a planar diffusion of tin formed the n^+ source and drain regions. Isolated low-leakage diodes were obtained. Very little conductivity enhancement was observed, even for gate fields approaching the dielectric breakdown of the silicon dioxide (5×10^6 V/cm). This behaviour was attributed to a high state density at the interface between the gallium arsenide and the silicon dioxide.

In a depletion-type transistor, the field is required merely to modulate the density of majority carriers. Therefore, the only interface states which affect the gate field are those near the conduction-band edge. For this reason, subsequent major effort was concentrated on depletion-type units,

although the fabrication process includes a critical channel diffusion.

SEMICONDUCTOR–OXIDE SYSTEM

MOS surface varactors were fabricated and their capacitance–voltage characteristic analysed[2] to determine the best combination of crystal orientation, surface treatment, and oxide-deposition

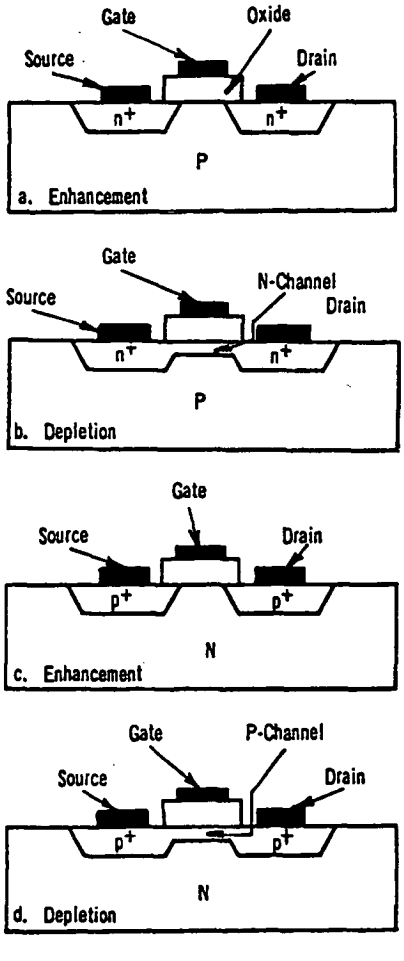

Fig. 1. MOS structures. (*a*) and (*b*) *n*-channel; (*c*) and (*d*) *p*-channel.

process. Although it is difficult to obtain specific information about the distribution of interface states from this type of measurement, it is possible to estimate the average fast-state density (states responding in the order of seconds or less), the equilibrium interface voltage, and the fraction of fast states responding to the 1 Mc test frequency used. It was found that there are a number of combinations which reduce the state density of pyrolytically deposited silicon dioxide on *n*-type gallium arsenide to the low range of 10^{12} states/cm^2/V. The method chosen was a rapid (approximately 1 to 2 min) high-temperature (730°C) deposition on the untreated chemically polished ($\bar{1}\bar{1}\bar{1}$) plane; this method yielded the most reproducible results.

It was also observed in all cases that the direction of the equilibrium interface voltage was such that the majority carrier density was reduced at the interface. Figure 2 shows in a qualitative manner typical capacitance–voltage characteristics and corresponding band diagrams at zero bias for MOS surface varactors fabricated on *n*- and *p*-type gallium arsenide. The dotted lines in the figure illustrate the effect of vacuum baking for 16 hr at 800°C. These baking conditions were investigated because it is standard procedure to heat-treat pyrolytically deposited films immediately after deposition. The heat treatment reduces the dielectric constant and dissolution rate of the film to values comparable to those of thermally grown oxide on silicon. Baking has very little effect on the state density, but changes the equilibrium surface voltage and causes the shift shown in the C–V characteristics.

TRANSISTOR PROCESSING

Figure 3 shows a gallium arsenide MOS transistor at various stages of processing. Gallium arsenide wafers (*p*-type) having an acceptor concentration (Cd or Zn) from 2 to 8 × 10^{16} carriers/cm^3 are lapped and chemically polished on the arsenic ($\bar{1}\bar{1}\bar{1}$) face. A silicon dioxide layer approximately 1700 Å thick is then deposited by means of a fast pyrolytic deposition method similar to the method originally described by JORDAN.[3] A schematic diagram of the system is shown in Fig. 4. In this deposition technique the wafer is placed on a quartz work platform in the centre of a horizontal quartz tube furnace which is then heated to 600°C while flushing with argon. Tetraethoxy silane vapor is then introduced by passing argon through the source bubbler at a flow rate of 850 cm^3/min. It is important to start the deposition at a sufficiently low temperature so as to obtain an oxide coating which will prevent the gallium arsenide surface from dissociating at the

higher temperatures. The temperature of the furnace is rapidly increased to 730°C and maintained until the desired film thickness is obtained (1 min for 1700 Å). The deposition is terminated by flushing the tube with argon until the sample is removed at 300°C.

The oxide-coated wafer is then heat-treated in vacuum, and the source and drain regions are opened by use of standard photoresist techniques. The geometry used in this investigation was a source, drain, and channel simultaneously. The diffusion is performed in an evacuated quartz ampoule, with time and temperature set to obtain a source and drain junction depth of about 4000 Å with a surface concentration of 10^{19} carriers/cm^3 and a channel depth of less than 1000 Å with a surface concentration of about 10^{17} carriers/cm^3. At this point, the electrical characteristics of the devices are checked. The drain-to-substrate reverse breakdown voltage is generally between 8 and 10 V

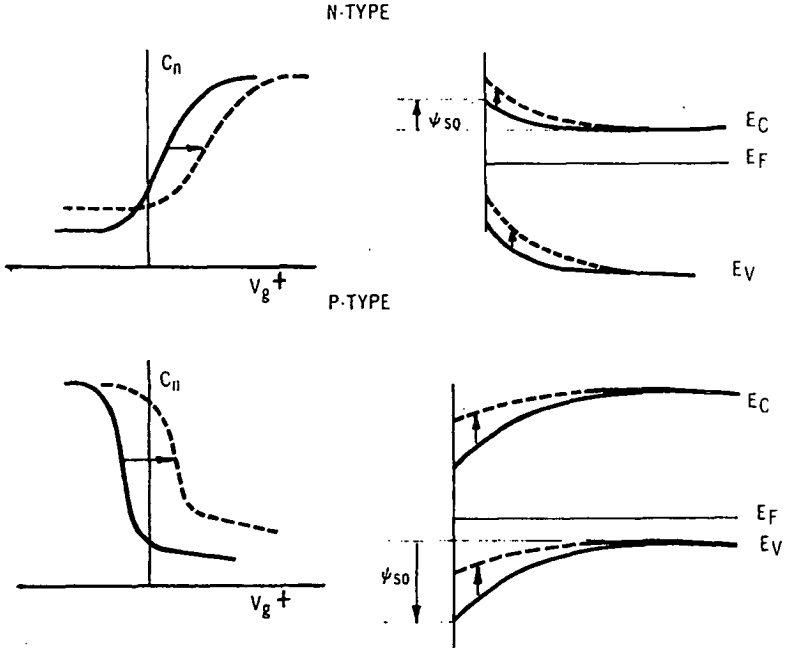

Fig. 2. Typical C–V characteristics and zero-bias energy-band diagrams for silicon dioxide–gallium arsenide MOS surface varactors. – – – Effect of 16 hr, 800°C vacuum brake.

simple rectangular structure having a channel length of 7 μ, a channel width of 126 μ, and a W/L ratio of 18 to 1. For the critical point of the process, obtaining the correct channel diffusion depth and concentration, a special diffusion technique developed for producing low-surface-concentration n-type diffusions is used. This technique utilizes the partial masking of the diffusant by a sufficiently thin (< 600 Å) silicon dioxide layer applied over the channel region.

Tin is used as the donor impurity to form the at 10 μA, and the source-to-drain saturation current is very high (approximately 50 mA). In many cases, breakdown occurs before saturation.

The oxide for the gate insulation is then deposited in the same manner used previously. A heat treatment follows, and the oxide over the source and drain regions is then opened for contacts. Electrical probing at this point shows a marked decrease in saturation current and an increase in breakdown voltage. The decrease in saturation current can be attributed to an increase in negative

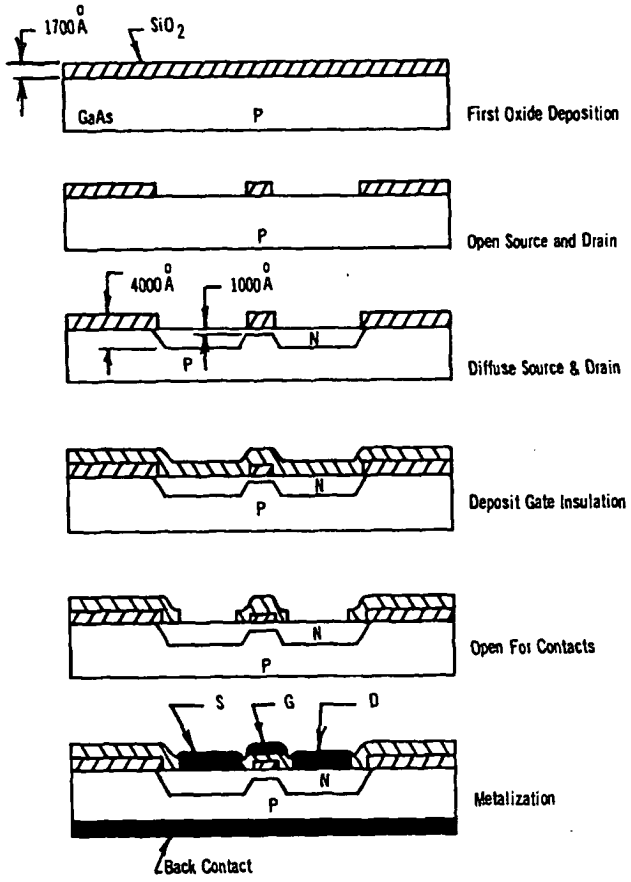

Fig. 3. Cross-section of a MOS unit at various processing stages.

charge in the oxide which causes partial depletion of the channel and a decrease in surface concentration due to the redistribution and outdiffusion of tin, the latter effect accounting for the increased breakdown voltage.

Contacts are applied to the source, drain and gate by evaporation of silver, and then are sintered. The wafer is scribed into individual pellets, and the pellets are mounted on TO-18 headers with lead used as the mounting material. Gold wires 0·5 mil dia. are then thermocompression bonded to the source, drain, and gate to complete the structure. The device is encapsulated in a dry nitrogen atmosphere.

ELECTRICAL CHARACTERISTICS

Table 1 gives the characteristics of ten units fabricated by means of the process described above. The units are listed in order of increasing saturation current, which varies over a wide range. The lower-current units 1, 2, 3, and 5 could be switched off with negative gate voltages less than 5 V. The typical substrate-to-drain breakdown voltage was 14 V at 40 μA. It is of interest to compare the zero-bias conductance g_0 with the gate transconductance g_m and the substrate transconductance g_{ms}. In all cases the transconductance from the gate is less than g_0, while the transconductance from the substrate is greater than or equal to g_0 except in the very-high-current devices.

The value of g_m was also measured as a function of frequency up to 5 Mc and was found to increase with increasing frequency. This increase is caused by a reduction in the number of interface states

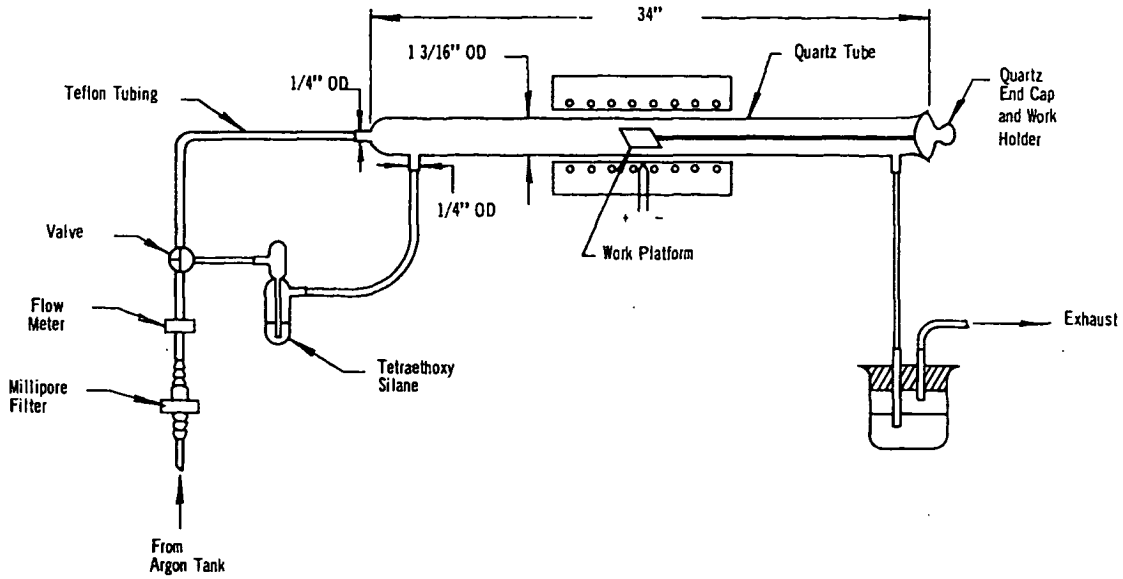

Fig. 4. Essential components of the silane deposition furnace.

Table 1. Characteristics of gallium arsenide MOS transistors

Unit no.	I_{d0} $V_g = 0$, (mA)	V_{d0} $V_g = 0$, (V)	$BV_{\text{Sub-D}}$ at 50μA, (V)	G_0 at Zero Bias (μ mhos)	g_m $f = 120$ c/s (μ mhos)	g_m(max) $f < 5$mc/s (μ mhos)	g_{ms} (Substrate control) (μ mhos)	$V_{g(\max)}$ (V)	V_{s0} (V)	μ_{avg} (cm^2/V sec)
1	0·05	1·0	13·5	100	30	42	140	15	4·5	170
2	0·05	1·0	15·0	90	20	22	90	15	4·0	90
3	0·10	0·7	16·2	200	37	202	240	15	4·0	1150
4	0·30	2·0	13·5	150	50	60	160	15	—	120
5*	0·40	1·5	15·0	500	240	—	—	15	4·0	640
6	0·50	1·5	16·0	450	50	130	450	15	—	350
7	4·50	6·0	11·8	600	250	750	1000	15	—	500
8†	≈16·0	≈10·0	10·3	2000	>700	—	>1000	15	—	>280
9†	≈20·0	≈10·0	10·2	2000	>700	—	>1000	15	—	>280
10*	25·0	4·5	11·8	9500	550	2000	4000	15	—	1780

* Units were destroyed during testing.
† Units did not saturate.

which respond to the applied signal as the frequency is increased.

Figure 5 shows transconductance as a function of frequency for several of the units listed in Table 1. This frequency performance indicates an appreciable state density in the range between 20 c/s and 1 Mc. The 6-db fall-off observed in the low-current devices at about 500 kc is caused by a high output time constant associated with the output capacitance and the high load resistance.

The last column of Table 1 shows average channel mobility μ calculated by use of the following formula

$$\mu_{avg} = \frac{g_m L}{V_{d0} C_{0x} W}. \qquad (1)$$

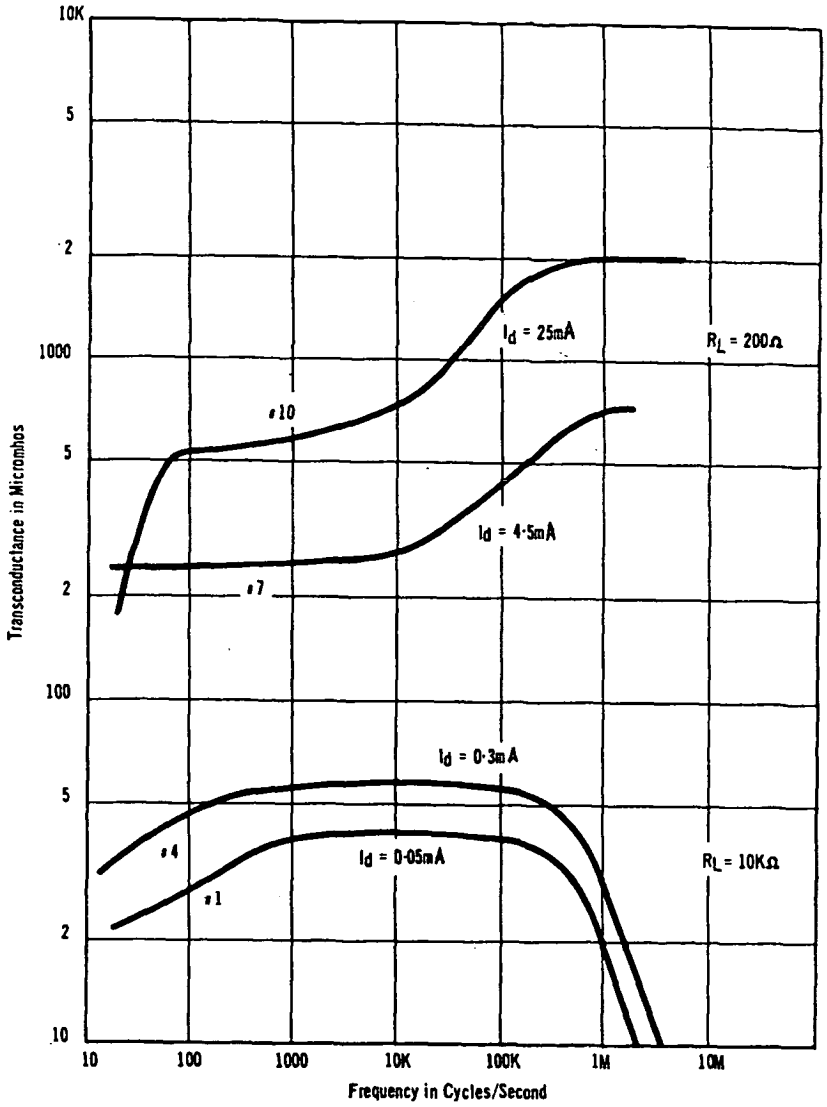

Fig. 5. Transconductance as a function of frequency for gallium arsenide MOS transistor.

This equation is easily derived if it is assumed that all the induced charges in the semiconductor material are mobile and move from source to drain at a constant velocity given by $\mu_{av0}v_{d0}/L$. The effect of interface states can be minimized by use of the maximum transconductance in the calculation.

Voltage–current characteristics of a typical low-current device in the enhancement and depletion modes are shown in Fig. 6. This device has a rather low saturation voltage and a high output resistance. The g_m is fairly linear in the enhancement mode. The device could be switched off with about 4·5 V. Two interesting effects are illustrated in the characteristics. The saturation current at zero gate voltage is not constant, but depends on the mean bias applied to the gate. The zero-bias saturation current is effectively zero in the enhancement

mode, but in the depletion mode it is about 80 μA. A looping of the trace is also observed. Both of these effects are believed to be associated with the charging and discharging of interface states.

Figure 7 compares the output characteristics of typical gallium arsenide and silicon MOS enhancement transistors of the same geometry. The gallium arsenide device exhibits a higher output impedance and, consequently, a greater voltage gain. In addition, its transconductance is nearly constant over the range considered, while the transconductance of the silicon device decreases rapidly at low currents. One reason for this tendency toward linear behaviour for the GaAs-device is that the saturation voltage is relatively independent of the applied gate voltage because the channel saturation is dominated by depletion from the substrate. If the average channel mobility is calculated (with allowance made for the difference in oxide thickness), the effective mobility is found to be 640 cm^2/V/sec for gallium arsenide and 200 cm^2/V/sec for silicon.

EFFECT OF SURFACE STATES ON MOS CHARACTERISTICS

A qualitative explanation of several of the observed characteristics and some knowledge of the effect of surface states were obtained from the physical model shown in Fig. 8. The channel, which is assumed to be uniformly doped, is shown under the zero-bias condition. It is depleted to a distance u_0 because of the built-in potential at the substrate-channel junction. The model also includes a depletion region of the oxide-channel interface. The existence of this region is evident from MOS capacitor characteristics. In the model it is assumed that this depletion is caused by fast states, which are distributed with uniform density over the forbidden gap; the effect of slow states is neglected.

When a voltage is applied to the drain with the gate tied to the source, electric fields are created across the gate oxide and the substrate-channel junction; these fields increase the depletion of the channel and thereby reduce the channel conductance. At saturation, the depletion from the substrate (u_s) just touches the depletion from the surface (v_s), and the conductivity of the channel approches zero. When the interface state density and substrate carrier concentrations are high, u_s is much greater than v_s and the saturation conditions are dominated by depletion from the substrate. This effect is evident in GaAs MOS transistors, where saturation conditions are much more dependent on the substrate voltage than on the gate voltage. This accounts for the relative independence of the transconductance with respect to gate bias. The equation derived from the model

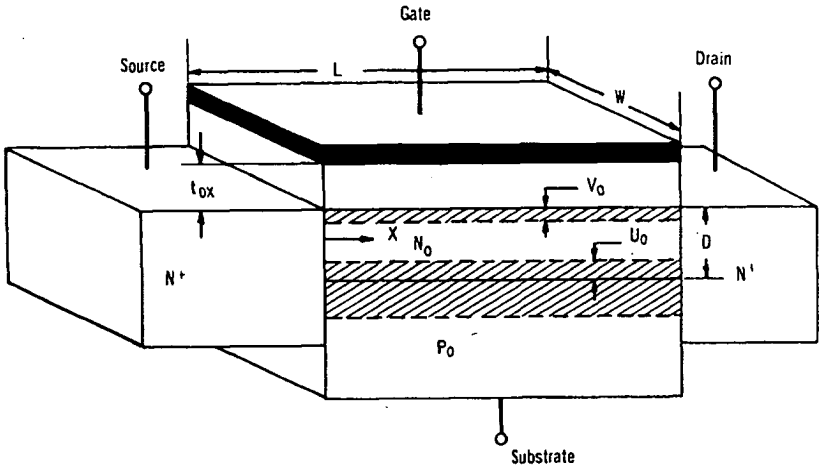

Fig. 8. Physical model for gallium arsenide MOS transistor.

of Fig. 8 in the Appendix in general involves too many unknown quantities to be directly applied. However, the relationships for the gate and substrate transconductance can be simplified at the zero-gate-bias conditions as shown below:

$$g_{ms}/g_0 = \frac{D-v_0-u_0}{D-v_0-u_0} = 1 \qquad (8)$$

$$g_m/g_0 = \frac{D-v_0-u_s}{D-v_0-u_0} < 1 \qquad (15)$$

Both these transconductances are closely related to the zero-bias conductance, the substrate conductance being always equal to or greater than g_0 and the gate transconductance less than g_0. Although these inequalities were generally valid for the ten units measured, there were one or two exceptions in each case. Equation (14) in the Appendix shows that the gate transconductance approaches zero for high interface state densities. This effect explains the increase in g_m with frequency because the effective state density is reduced as the frequency is increased.

CONCLUSIONS

A process has been developed which uses planar technology for the construction of gallium arsenide MOS transistors. Evaluation of these devices indicates that the effective channel mobility, although considerably below the expected bulk value, is higher than that observed for typical silicon MOS transistors. With the present devices, this advantage is not fully realized because of a relatively high state density at the interface between the gallium arsenide and the silicon dioxide. In MOS surface varactors used as test vehicles, it has been possible to reduce this density to about 1×10^{12} carriers/cm^2/V by optimization of the process conditions. However, a further reduction by an order of magnitude is necessary before the effect of these states is negligible.

A model similar to that proposed by SHOCKLEY[4] for the field-effect transistor has been used to investigate the effect of fast states on the characteristics of the device.

Acknowledgements—The authors wish to thank D. BERGMAN, D. JACUKOWICZ, and J. MOONAN for their technical assistance on this project.

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APPENDIX: THEORY OF OPERATION

A model similar to that used for field-effect transistors[4] is proposed to account for the observed characteristics of n-channel depletion-type MOS transistors. The voltage–current characteristic is calculated for the case of a uniformly doped n-channel region on the surface of a p-type semiconductor. When a voltage is applied to the drain, electric fields are created across the gate oxide and the substrate-channel junction. These fields terminate on ionized donors in the channel region and thereby reduce the channel conductance. If surface states exist, the gate field partially terminates at surface charges and is less effective in reducing the channel conductance. As the drain voltage is increased, the depletion of the channel continues until the current flows in a thin plane. The channel conductance is then very small and the channel current saturates. The channel saturation current may be varied by biasing either the gate or the substrate.

(a) *Substrate control—no metal gate*

The effective cross section, a, at a distance x from the source is

$$a = W(D-v_0-u)$$

where v and u represent the depletion regions into the channel from the oxide-semiconductor interface and the substrate channel junction respectively. In this case the total channel depth D is only of the order of 1000 Å and the effect of v and u cannot be neglected as in the Shockley model.

The source-to-drain current I_d may be expressed in terms of the field E_x and the conductivity σ as follows:

$$I_d = a\sigma E_x = -\sigma\frac{dV_{(x)}}{dx}(D-v_0-u)W \qquad (2)$$

However, u and V are related by Poisson's equation for the reversed-bias junction; therefore it is given by

$$u = \left[\frac{V_{(x)}-V_s+\phi}{A(1+N_0/P_0)}\right]^{1/2} \qquad (3)$$

where ϕ is the built-in voltage between the channel and substrate, $A = qN_0/2\epsilon$ and V_s is the applied voltage between source and substrate. If equation (3) is substituted into equation (2) and the result integrated, the drain current is obtained as a function of the drain voltage V_d

and the substrate voltage V_s, as follows:

$$I_d = -\frac{\sigma W}{L} \times \left\{(D-v_0)V_d - \frac{2}{3}\frac{(V_d - V_s+\phi)^{3/2}-(\phi-V_s)^{3/2}}{[A(1+N_0/p_0)]^{1/2}}\right\} \tag{4}$$

The zero-bias conductance g_0 is given by

$$g_0 = \frac{\sigma W}{L}(D-v_0-u_0) \tag{5}$$

For this value of g_0 and at the saturation conditions $I_d = I_{d0}$ and $V_d = V_{d0}$, equation (4) may be written as follows:

$$I_{d0}/g_0 = -\left(\frac{D-v_0}{D-v_0-u_0}\right)V_{d0} + \frac{2}{3}\frac{(V_{d0}-V_s+\phi)^{3/2}-(\phi-V_s)^{3/2}}{(D-v_0-u_0)[A(1+N_0/p_0)]^{1/2}} \tag{6}$$

This equation may be differentiated with respect to V_s, to yield the following relationship for transconductance g_{ms} with substrate control:

$$g_{ms} = -\frac{\partial I_{d0}}{\partial V_s} = \frac{g_0}{D-v_0-u_0} \times \left\{\left[\frac{V_{d0}-V_s+\phi}{A(1+N_0/p_0)}\right]^{1/2} - \left[\frac{\phi-V_s}{A(1+N_0/p_0)}\right]^{1/2}\right\} \tag{7}$$

By use of equation (3) at the saturation condition, equation (7) can be simplified as follows:

$$g_{ms}/g_0 = \frac{D-v_0-u_0}{D-v_0-u_0} = 1 \tag{8}$$

Equation (8) is equivalent to the Shockley result. This analysis, however, neglects series resistances which may exist in the source and drain contact regions. Therefore, in general the measured zero-bias conductance will be smaller than the substrate transconductance.

(b) *Gate control*

If a metal gate electrode is deposited over the channel region, the saturation current is reduced because the metal, which is an equipotential surface, causes an increased self-depletion at the drain end of the channel and a reduced self-depletion at the source end.

The source-to-gate voltage V_g may be expressed as follows:

$$V_g - V_{(x)} = V_{0x}+\psi_s-\psi_{s0} \tag{9}$$

$$= -\frac{Q_{sst}+Q_s}{C_{0x}}+\psi_s-\psi_{s0} \tag{10}$$

where ψ_{s0} is the surface potential of the semiconductor under no bias,
ψ_s is the surface potential of the semiconductor,
Q_{sst} is the charge in the surface states, and
Q_{st} is the charge in the space-charge region of the semiconductor.

The charge in the surface states is generally a complicated function of the surface voltage. However, the simplifying assumption of a linear dependence makes it possible to obtain qualitative information on the influence of high state density on transconductance. If the following assumption is made:

$$Q_{sst} = Q_0 - qK\cdot\psi_s \tag{11}$$

then substitution of equation (11) into (10) produces the following result:

$$V_g - V_{(x)} = -\left(1+\frac{qK}{C_{0x}}\right)\cdot Av^2 - \frac{qN_0}{C_{0x}}\cdot v - \left(\frac{Q_0}{C_{0x}}+\psi_{s0}\right) \tag{12}$$

where it is assumed that the surface is sufficiently depleted that the depletion depth v may be related to ψ_s and Q_{st} by the approximate expressions:

$$v^2 = -\psi_{s/A}$$

and

$$Q_{st} = qN_0v.$$

The parameters m, t, and V_0 are defined as follows:

$$m = C_{0x}/(C_{0x}+qK)$$

$$t = \epsilon/C_{0x}$$

$$V_0 = Q_0/C_{0x}+\psi_{s0}$$

The depletion depth v is then given by

$$v = \left[m^2t^2+\frac{m}{A}(V_{(x)}-V_0-V_g)\right]^{1/2} - mt \tag{13}$$

The channel current may be obtained by substituting v for v_0 in equation (2) and integrating with respect to x.

Differentiation of the resulting expression for I_{d0} at the saturation conditions with respect to the gate voltage

V_g yields the following result:

$$g_m = -\left(\frac{\partial I_{d0}}{\partial V_g}\right)_{V=V_{d0}} = \frac{\sigma W}{L}\left\{\left[m^2t^2+\frac{m}{A}(V_{d0}-V_0-V_g)\right]^{1/2} - \left[m^2t^2-\frac{m}{A}(V_0+V_g)\right]^{1/2}\right\} \quad (14)$$

By inspection it is seen that the transconductance is dependent on the parameter m, which is a function of the surface-state density K. As K approaches infinity, m approaches zero and the transconductance g_m also approaches 0.

At the zero-bias condition (i.e. $V_g = 0$), equation (14) may be rewritten as follows:

$$g_m = \frac{\sigma W}{L}(D-v_0-u_s)$$

where u_s is the value of u (at $x = L$) at saturation, or

$$g_m/g_0 = \frac{D-v_0-u_s}{D-v_0-u_0}; \qquad u_s > u_0 \quad (15)$$

Thus it is seen that g_m is always less than or equal to g_0. One then may conclude that for a low carrier concentration in the substrate, in which case u_s approaches u_0, the highest gate-transconductance is achieved.

Rick –

Signed copy of declaration by Mark Johnson.

(1) On page 3, section 13, last sentence, 6th word, should have been "in" → signed copy rather than "is" → draft

(2) Copy of Fountain, et al. attached. They include C-V data as would be expected. in analysis of a gate oxide.

– Mark

ATTACHMENT 7

2

IN RE APPLICATIONS OF: DAVID BRADDOCK

37 CFR 1.132 DECLARATION OF MARK JOHNSON

1. I am an assistant professor in the Department of Materials Science and Engineering at NC State University. I specialize in semiconductor devices, particularly III-V semiconductor devices. I am an expert in that field.

2. I've taken an look the following materials:

3. US patent 5,945,718 naming Passlack et al. as inventors.

4. NEIFELD Docket No.: OSEM-DB12

Claim 45. A complementary metal-oxide compound semiconductor integrated circuit comprising an enhancement mode metal-oxide-compound semiconductor field effect transistor, said transistor comprising;

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on said upper surface, said gate structure comprising an adjacent layer comprising indium, gallium, and oxygen, said adjacent layer being adjacent said upper surface of said compound semiconductor wafer structure;

a gate electrode positioned on said upper surface;

source and drain self-aligned to the gate electrode;

source and drain ohmic contacts positioned on source and drain areas, wherein said compound semiconductor wafer structure comprises a wider band gap spacer layer and a narrower band gap channel layer;

wherein said narrower band gap channel layer comprises InyGa1-yAs; and

wherein said transistor is integrated together with similar or complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuit.

5. NEIFELD REF: OSEM-DB13

Claim 45. A complementary metal-oxide compound semiconductor integrated circuit comprising an enhancement mode metal-oxide-compound semiconductor field effect transistor, said transistor comprising;

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on said upper surface;

a gate electrode positioned on said gate insulator structure;

source and drain self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on source and drain areas of said source and drain;

wherein said compound semiconductor wafer structure comprises a wider band gap

spacer layer and a narrower band gap channel layer;

wherein said narrower band gap channel layer comprises InyGa1-yAs; and

wherein said transistor is integrated together with similar or complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuit.

6. I have been told that David Braddock applied for patents containing these claims. I am generally familiar with David Braddock's device structures, although I do not know epitaxial growth or gate oxide deposit processing details.

7. I have ben told that the patent examiner rejected the two claims recited above as anticipated by the disclosure in US patent 5,945,718.

8. I have been told that the patent examiner assumed that the stoichiometric Ga2O3 layer disclosed in US patent 5,945,718. was a "gate insulator structure" as defined in the foregoing two claims.

9. I have been told that the examiner assumed that US patent 5,945,718 disclosed a "enhancement mode metal-oxide-compound semiconductor field effect transistor. That is, an enhancement mode MOSFET (Metal-Oxide Semiconductor Field Effect Transistor), as defined in the foregoing two claims.

10. I have been told that the examiner assumed that disclosed the "metal-oxide-compound semiconductor field effect transistor" as defined in the foregoing two claims.

11. The examiners assumptions regarding 5,945,718 just noted are all incorrect. US patent 5,945,718 does not disclose a MOSFET, does not disclose a gate insulator structure of a MOSFET, and does not disclose a MOSFET device capable of enhancement mode operation. In fact, US patent 5,945,718 discloses a MISFET (Metal-Insulator Semiconductor Field Effect Transistor) HEMT structure, not a MOSFET. The MISFET disclosed in US patent 5,945,718 contains both a metal and an oxide layer. US patent 5,945,718 does not describe a MOSFET as it would be generally recognized by semiconductor researchers. MISFETs have gate insulator, but their range of enhancement mode operation is usually over a limited gate voltage. Accordingly, the patent examiner's assumptions are all wrong.

12. My opinion is based on the following considerations:

13. Generally speaking, for a structure to be considered a MOSFET by one skilled in the art, it must satisfy certain performance criteria relating to the electrical properties that define a MOSFET. These include certain information such as current-voltage (IV) characteristics of the source to gate electronic transport (leakage current/unit area) and capacitance-voltage (CV) characteristics of the source to gate electric field pathway (gate capacitance/unit area). Values for these two metrics define whether the structure is in fact a MOSFET. These two metrics are

routinely used to evaluate quality of and determine the characteristics of MOSFET structures fabricated from the Silicon/Silicon-Dioxide material system by those skilled in the art, including Dr. Passlack's own organization, Motorola. Failure to include such data in the disclosure of US patent 5945718 raises a red-flag to any expert at MOSFET technology as to whether the disclosed structure in that patent is a MOSFET, rather than just a MISFET.

14. A MOSFET structure for GaAs semiconductors specifically and compound semiconductors in general has been a goal of the semiconductor industry since 1965 (Becke, Hall and White). The research and development related to a suitable gate oxide on compound semiconductors is notable for the failures. Several excellent review have been written of these attempts including (Croydon, 1981) and (Wilmsen, 1985). A typical result reported in this technical art would be that of (Fountain, Rudder, Hattangaty, Makunas and Hutchby, 1989) who claim a MISFET rather than a MOSFET (Metal-Oxide Semiconductor Field Effect Transistor) for their work despite the fact that it contained a oxide insulator. The work by (Fountain, et. al.) contained multiple semiconductor layers, as does that of Passlack. As a result of the long-standing history of compound semiconductor MOSFET research, those skilled in the art differentiate results as being (a) Very skeptical regarding the generalization of any claims or structures beyond the specific materials and structures disclosed, and (b) Differentiate more general MISFET device from MOSFET characteristics.

15. In US patent 5,945,718 figure 1 and the related description, the structures defined contains a semiconductor insulator layer (layer 15). Such a heterojunction layer is routinely grown by those skilled in the art of compound semiconductor field effect transistor fabrication, and is commonly referred to as a "gate layer." The semiconductor structure described is referred to as a heterojunction field effect transistor (HFET) or High Electron Mobility Transistor (HEMT). As well as acting as a source of electrons, when depleted, the donor layer in such structures acts as a gate insulator. The gate for such a structure is a metal deposited directly upon the semiconductor surface and forming a rectifying Schottky-Contact. When biased appropriately, the Schottky contact blocks the flow of electrons between the semiconductor and the metal, while providing a means of controlling the electric field shape in the underlying semiconductor material. This is the mechanism of modulating current in existing H-FET devices and is commonly referred to as a MESFET (Metal-Semiconductor Filed Effect Transistor) and is commonly used in device research as well as currently manufactured semiconductor HEMT or HFET products. Most HEMT or HFET devices have a limited range of enhancement mode operation. With appropriate design of the gate layer(15), donor layer (23) and channel layer (24) the HFET may be designed such that there is no flow of current between the source and drain (Id=0) while the gate is unbiased (Vg=0). The only observed DC conductivity would be the limited range of enhancement mode operation. This would be normal for a MISFET device which is designed to be 'normally -off' and might be referred to as an enhancement mode MISFET as opposed to an enhancement mode MOSFET. In fact, I conclude that all of the US patent 5945718 enhancement mode behavior is due to the structure disclosed therein being a HEMT/MISFET, and not necessarily a MOSFET.

16. Dr. Passlack has subsequently disclosed that Ga2O3, the material he claims in US patent 5,945,718 to be using as a gate oxide, is in-fact an n-type semiconductor. This is completely consistent with my conclusion that the device described in US patent 5,945,718 is a MISFET, similar to that described by (Fountain, 1989). The gate insulation in this structure is caused by the Schottky barrier formed at the interface between the Ga2O3 (layer 14) and GaAs (layer 15) coupled with the insulation provided by the undoped-GaAs in a MISFET structure (layer 15). The control electrode (17) is merely a source of electrons for this complex insulating gate structure, with the possibility of slight contact resistance or rectification between the gate metal (17) and the Ga2O3 (14) which is an n-type semiconductor according to Passlack's own subsequent publications. Thus, I consider Passlack's structure disclosed in US patent 5945718 to be a MISFET, not a MOSFET.

17. To reiterate, Passlack has described in US patent 5945718 a very intriguing MISFET structure which contains both a metal and an oxide layer on a semiconductor channel. He has not provided in US patent 5945718 an adequate degree of information to describe a MOSFET as it would be generally recognized by semiconductor researchers.

18. I swear under penalty of perjury of the laws of the United States that I believe that the foregoing is true and correct.

July 4, 04
DATE

MARK JOHNSON

Date/time: June 29, 2004 (6:01pm)
Y:\Clients\Osemi\OSEM_DB12\Drafts\MarkJohnsonDeclaration_040625.wpd

Demonstration of an n-Channel Inversion Mode GaAs MISFET

G.G. Fountain, R.A. Rudder, S.V. Hattangady, R.J. Markunas, J.A. Hutchby
Research Triangle Institute, PO 12194
Research Triangle Park, NC 27709 ,USA

An operational GaAs inversion mode n-channel MISFET has been demonstrated for the first time, using a composite SiO_2 (15 nm)/Si (1 nm)/GaAs structure. This result is based on an in situ hydrogen cleaning process (used to prepare the GaAs surface just prior to the Si/SiO_2 deposition), a low temperature pseudomorphic Si deposition process, and a low temperature high quality SiO_2 deposition process, all performed sequentially in an ultra high vacuum/load locked system.

It is well known that an oxidized GaAs surface has its Fermi level pinned near midgap. However, vacuum cleaved GaAs surfaces exhibit unpinned behavior. The key to fabrication of a low interface state MIS structure on GaAs is to prepare a stoichiometric, contamination free surface, and then preserve that surface throughout the processing. We have demonstrated through Auger and and x-ray photoemission spectroscopies (XPS), that both Ga and As oxides can be removed from the GaAs surface with carefully controlled activated hydrogen treatments. Reflecting high energy electron diffraction has been used to qualify the structure of GaAs surface after the hydrogen treatment. Furthermore, it has been demonstrated by XPS that a thin (1 nm) crystalline Si layer deposited by remote plasma enhanced CVD at 300°C, can be used to protect the surface of the GaAs from oxidation. An MIS structure can thus be fabricated by capping the Si layer with a low temperature high quality SiO_2 insulator. Thus any surface oxidation which occurs during the oxide deposition is accommodated by the Si and not the GaAs. The SiO_2 material used has been thoroughly qualified on Si, exhibiting interface state densities as low as $1 \times 10^{10} cm^{-2} eV^{-1}$ and breakdown fields of 10 MV cm^{-1}. This composite MIS technology has been incorporated into GaAs n-channel inversion mode MISFET structures fabricated on p-type GaAs ($1 \times 10^{15} cm^{-3}$) with Si implanted source-drain regions. The first working devices exhibit a DC transconductance of 0.26 mS/mm at a gate length and width of 2 microns and 50 microns, respectively (Figure 1). The threshold voltage is typically 1.5 volts. The transconductance is limited currently by a severe source drain resistance problem. Capacitance voltage analysis of MIS capacitors on chip with the transistors (Figure 2) indicates that the midgap electron trap density is on the order of $4 \times 10^{11} cm^{-2}$. This electron trapping density is manifested by a hump in the quasistatic CV characteristics, and appears from band bending analysis to be located at 0.7 eV above the valence band. Functioning FET devices have accompanied the reduction of this trapping level.

Band bending calculations have previously suggested that inversion of the GaAs surface had been achieved. The working inversion mode MISFET corroborates this result. The ability to invert the GaAs surface opens the possibility to a new class of high speed GaAs FET devices with the desirable features of enhancement mode insulated gate transistors.

9

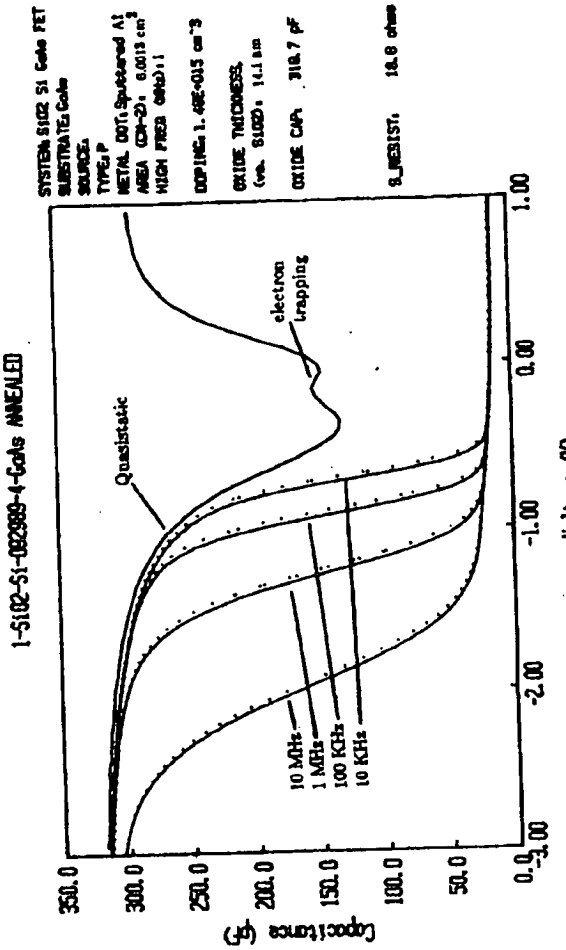

Figure 2. Multi-frequency CV characteristics of SiO_2/Si/GaAs MIS capacitors on chip with the MOSFET from Figure 1.

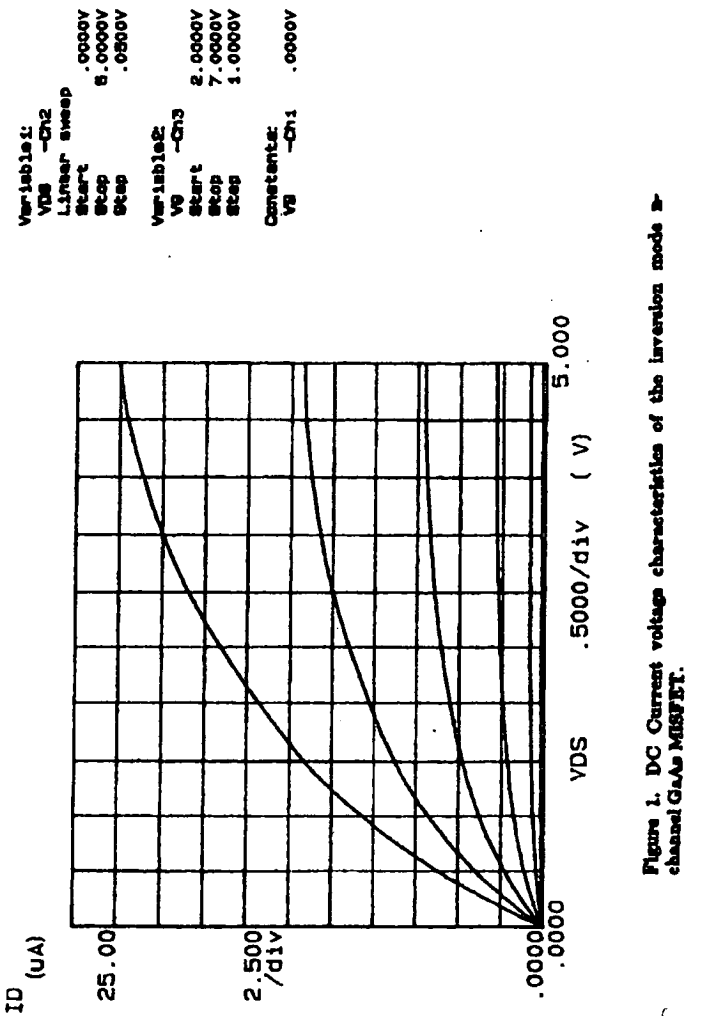

Figure 1. DC Current voltage characteristics of the inversion mode n-channel GaAs MISFET.

Materials

Accuflect
Aluminum Nitride
Aluminum Oxide
Boron Nitride
Fused Silica
Macor
Mullite
Sialon
Silicon Carbide
Silicon Nitride
Zirconium Oxide

Fused Silica, SiO_2

Fused silica is a noncrystalline (glass) form of silicon dioxide (quartz, sand). Typical of glasses, it lacks long range order in its atomic structure. It's highly cross linked three dimensional structure gives rise to it's high use temperature and low thermal expansion coefficient.

Key Properties

- ✓ Near zero thermal expansion
- ✓ Exceptionally good thermal shock resistance
- ✓ Very good chemical inertness
- ✓ Can be lapped and polished to fine finishes
- ✓ Low dielectric constant
- ✓ Low dielectric loss
- ✓ Good UV transparency

Typical Uses

- ✓ High temperature lamp envelopes
- ✓ Temperature insensitive optical component supports
- ✓ Lenses, mirrors in highly variable temperature regimes
- ✓ Microwave and millimeter wave components
- ✓ Aeronautical radar windows

General Information

High purity sand deposits provide the raw material for bulk refractory grade, which is electric arc melted at extremely high temperatures. Optical and general purpose fused silica rods and tubing are drawn from a melt made from high purity chemicals. Fiber optic purity is made by thermal decomposition of high purity gaseous silica containing chemicals. The glass may be clear or translucent, in which case it is often referred to as fused quartz. The glass has very high viscosity, and this property allows the glass to be formed, cooled and annealed without crystallizing. Fused silica glass is a very low thermal expansion material, and so is extremely thermal shock resistant. The material is also chemically inert up to moderate temperatures except to hydrofluoric acid, which dissolves silica. It will devitrify above about 1100°C in the presence of contaminants such as sodium, phosphorus and vanadium, with the formation of cristobalite crystals which destroy the properties of the glass. The dielectric properties are stable up through gigahertz frequencies.

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Engineering Properties*

Fused Silica

Attachment 8

Mechanical	Units of Measure	SI/Metric	(Imperial)
Density	gm/cc (lb/ft^3)	2.2	(137.4)
Porosity	% (%)	0	0
Color	—	clear	—
Flexural Strength	MPa ($lb/in^2 x10^3$)	—	—
Elastic Modulus	GPa ($lb/in^2 x10^6$)	73	(10.6)
Shear Modulus	GPa ($lb/in^2 x10^6$)	31	(4.5)
Bulk Modulus	GPa ($lb/in^2 x10^6$)	41	(6)
Poisson's Ratio	—	0.17	(0.17)
Compressive Strength	MPa ($lb/in^2 x10^3$)	1108	(160.7)
Hardness	Kg/mm^2	600	—
Fracture Toughness K_{1c}	$MPa \cdot m^{1/2}$	—	—
Maximum Use Temperature (no load)	°C (°F)	1100	(2000)
Thermal			
Thermal Conductivity	W/m•°K (BTU•in/ft^2•hr•°F)	1.38	(9.6)
Coefficient of Thermal Expansion	10^{-6}/°C (10^{-6}/°F)	0.55	(.31)
Specific Heat	J/Kg•°K (Btu/lb•°F)	740	(0.18)
Electrical			
Dielectric Strength	ac-kv/mm (volts/mil)	30	(750)
Dielectric Constant	@ 1 MHz	3.82	(3.82)
Dissipation Factor	@ 1 MHz	0.00002	(0.00002)
Loss Tangent	@ 1 MHz	—	—
Volume Resistivity	ohm•cm	$>10^{10}$	—

*All properties are room temperature values except as noted.
The data presented is typical of commercially available material and is offered for comparative purposes only. The information is not to be interpreted as absolute material properties nor does it constitute a representation or warranty for which we assume legal liability. User shall determine suitability of the material for the intended use and assumes all risk and liability whatsoever in connection therewith.

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Site Design M. Adams